FIG. 1

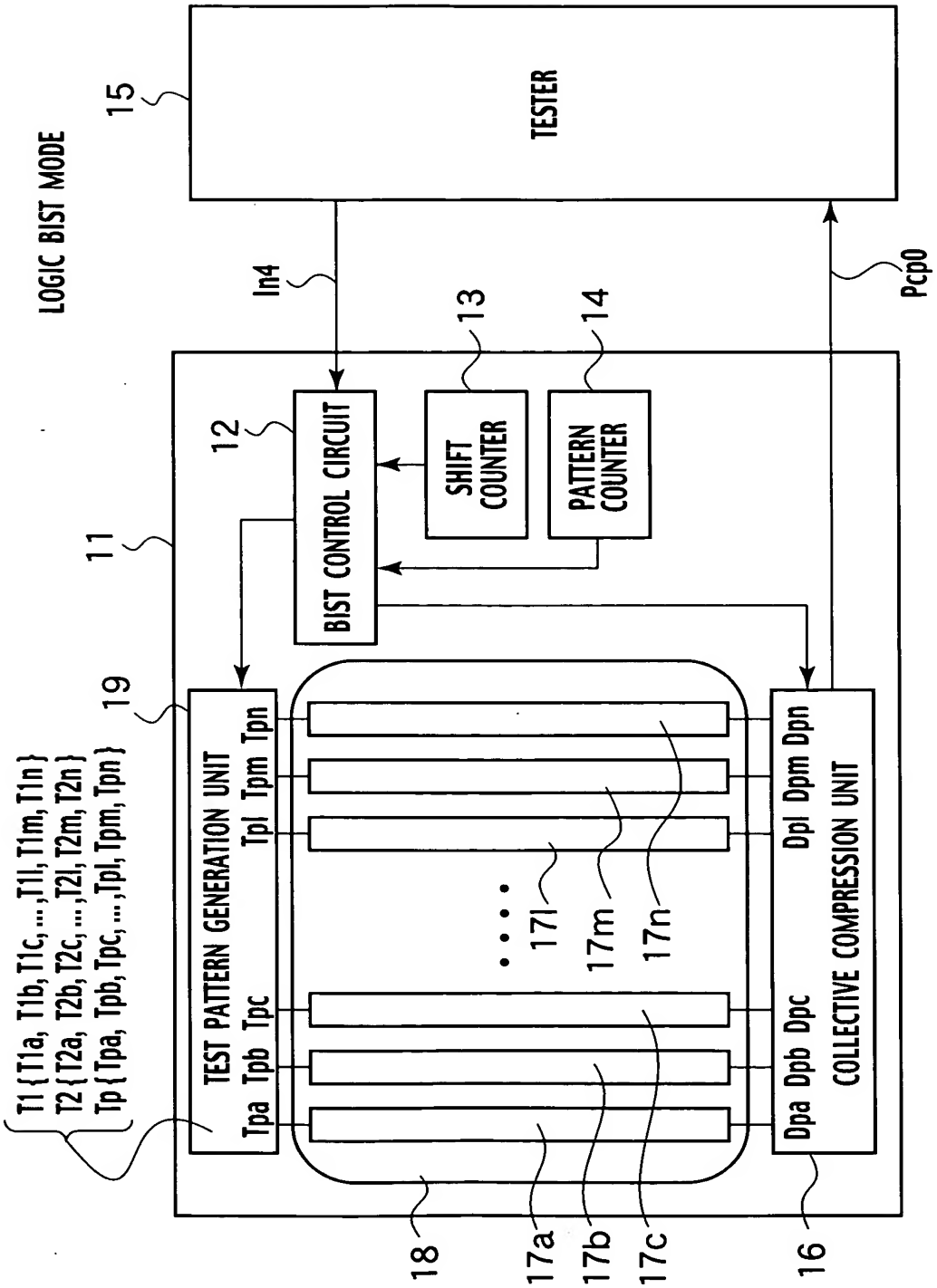

LOGIC BIST MODE
15
TESTER
In4
Pcp0
13
14
12
BIST CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
11
19
TEST PATTERN GENERATION UNIT
Tpa Tpb Tpc
Tpl Tpm Tpn
T1{T1a, T1b, T1c, ..., T1l, T1m, T1n}
T2{T2a, T2b, T2c, ..., T2l, T2m, T2n}
Tp{Tpa, Tpb, Tpc, ..., Tpl, Tpm, Tpn}
17l
17m
17n
Dpa Dpb Dpc
Dpl Dpm Dpn
COLLECTIVE COMPRESSION UNIT
18
17a
17b
17c
16

FIG. 2

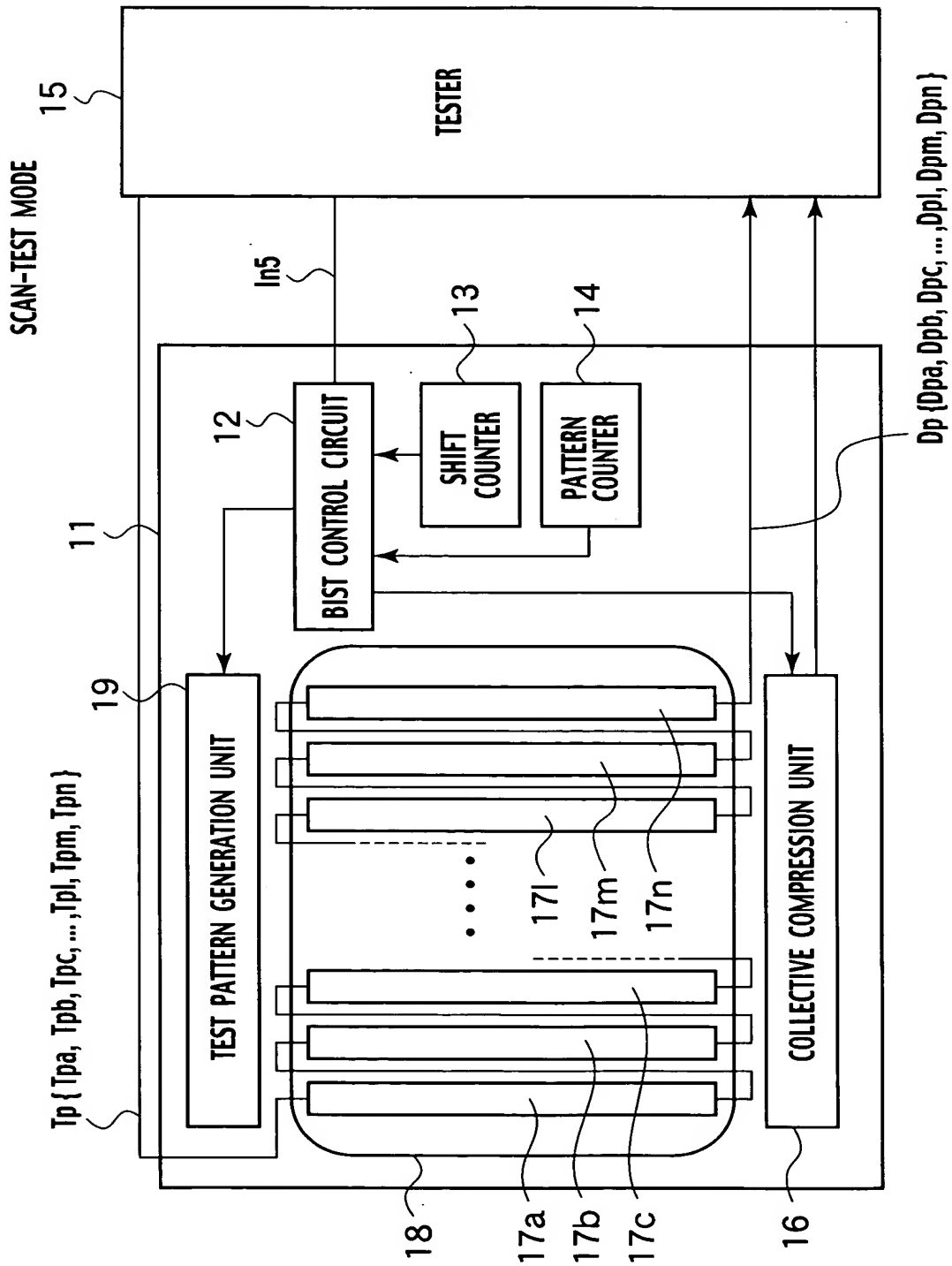

15
TESTER
SCAN-TEST MODE
In5
13
14
12
BIST CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
11
Dp {Dpa, Dpb, Dpc, ..., Dpl, Dpm, Dpn}
19
TEST PATTERN GENERATION UNIT
COLLECTIVE COMPRESSION UNIT
Tp {Tpa, Tpb, Tpc, ..., Tpl, Tpm, Tpn}
17l
17m
17n
18
17a
17b
17c
16

FIG. 3

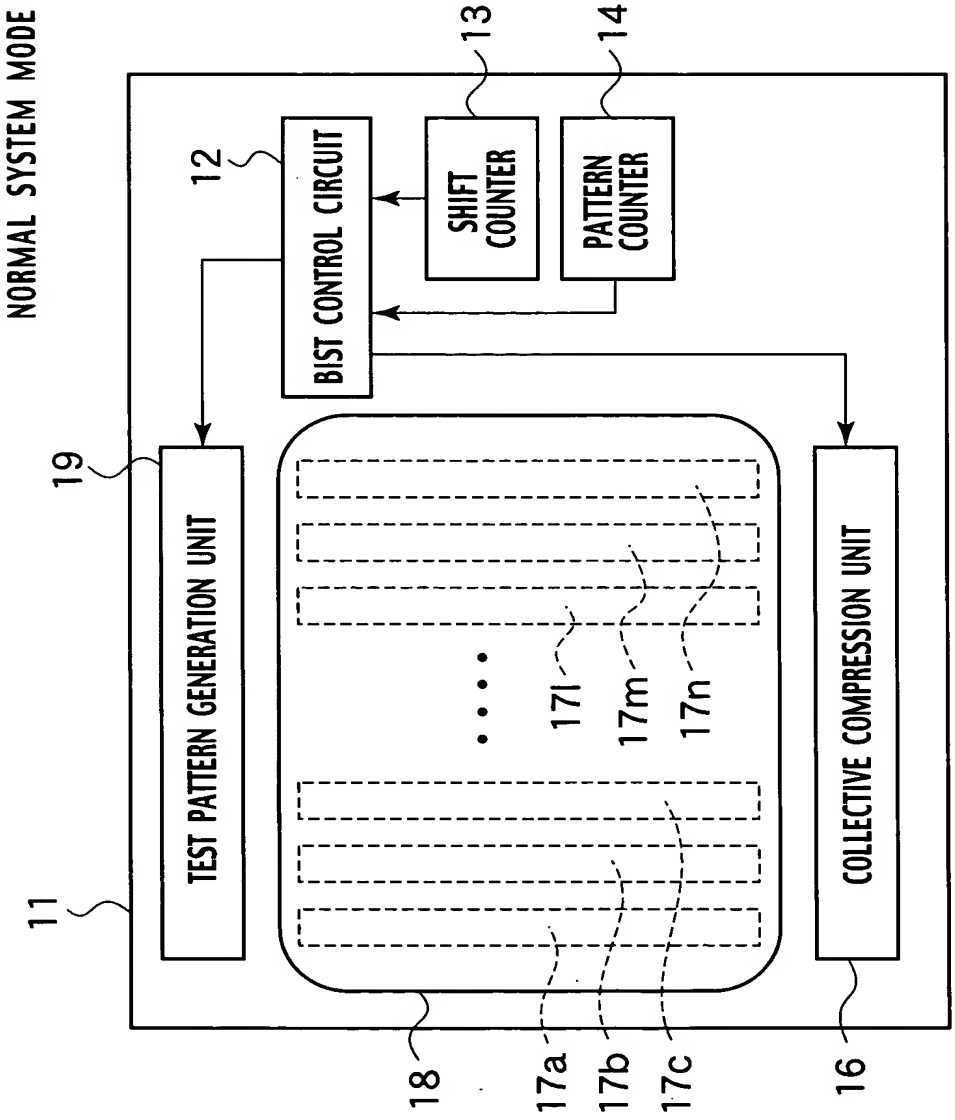

NORMAL SYSTEM MODE
11
12
13
14
16
17a
17b
17c
17l
17m
17n
18
19
BIST CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
TEST PATTERN GENERATION UNIT
COLLECTIVE COMPRESSION UNIT

FIG. 4

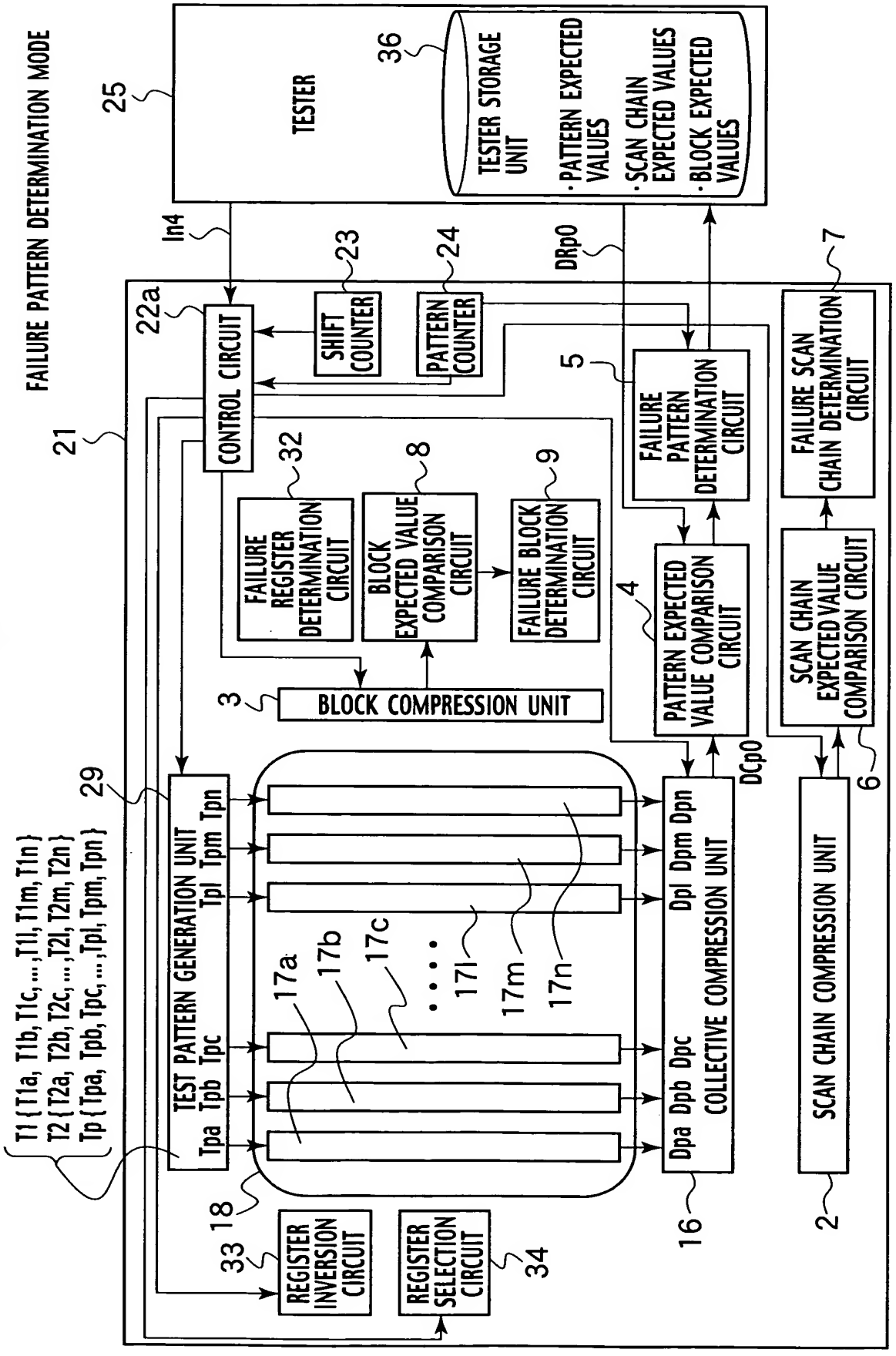

FAILURE PATTERN DETERMINATION MODE
25
TESTER
36
TESTER STORAGE UNIT
·PATTERN EXPECTED VALUES
·SCAN CHAIN EXPECTED VALUES
·BLOCK EXPECTED VALUES
In4
DRp0
23
SHIFT COUNTER
24
PATTERN COUNTER
7
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
22a
CONTROL CIRCUIT
5
FAILURE PATTERN DETERMINATION CIRCUIT
21
32
FAILURE REGISTER DETERMINATION CIRCUIT
8
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
9
FAILURE BLOCK DETERMINATION CIRCUIT
4
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
6
3
BLOCK COMPRESSION UNIT
DCp0
29
TEST PATTERN GENERATION UNIT
Tpa Tpb Tpc
Tpl Tpm Tpn
17a
17b
17c
17l
17m
17n
18
Dpa Dpb Dpc
Dpl Dpm Dpn
COLLECTIVE COMPRESSION UNIT
16
SCAN CHAIN COMPRESSION UNIT
2
33
REGISTER INVERSION CIRCUIT
34
REGISTER SELECTION CIRCUIT
T1{T1a, T1b, T1c, ..., T1l, T1m, T1n}
T2{T2a, T2b, T2c, ..., T2l, T2m, T2n}
Tp{Tpa, Tpb, Tpc, ..., Tpl, Tpm, Tpn}

FIG. 5

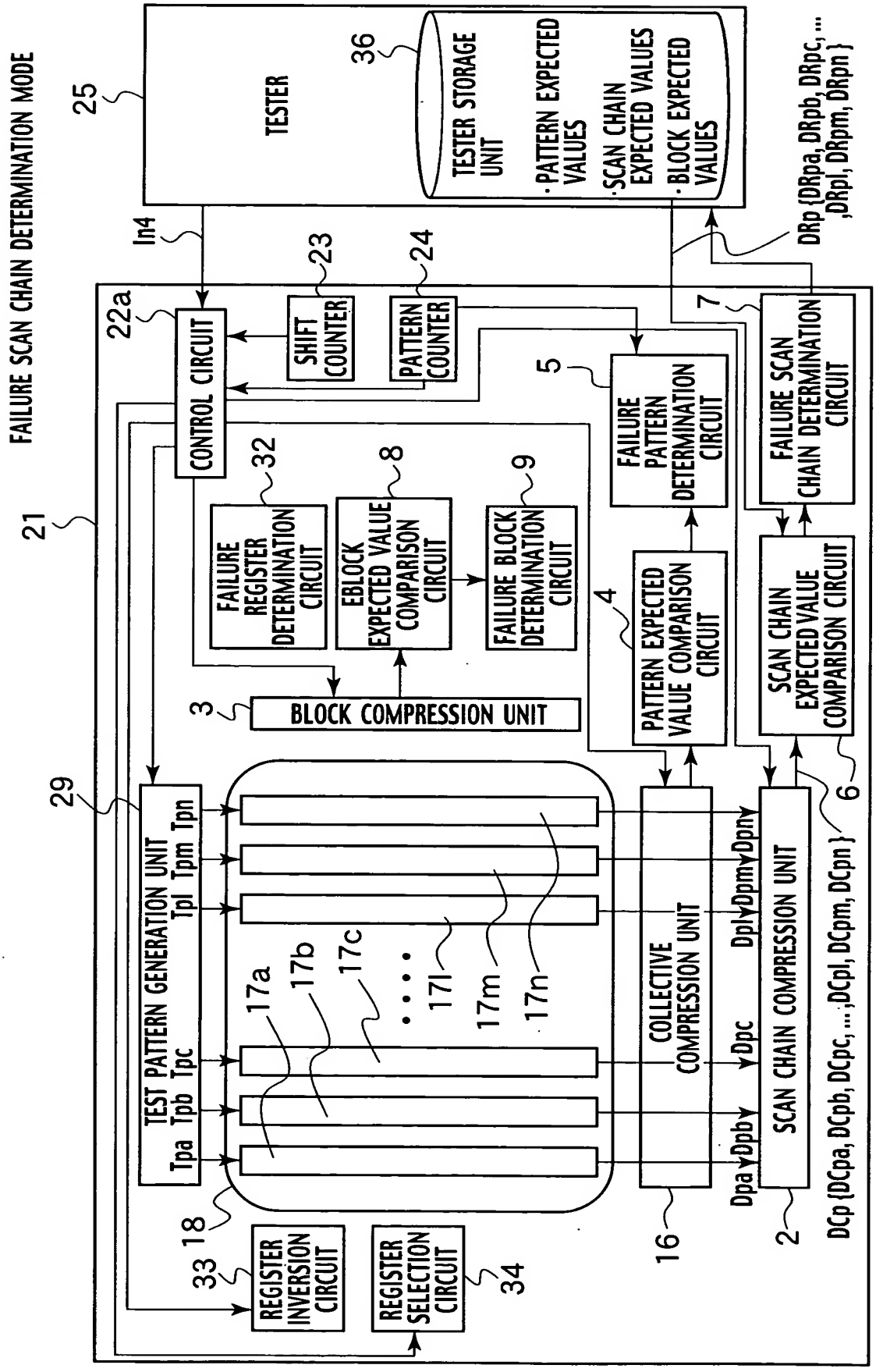

FAILURE SCAN CHAIN DETERMINATION MODE
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
·SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
DRp {DRpa, DRpb, DRpc, ... ,DRpl, DRpm, DRpn }
In4
CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
FAILURE PATTERN DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
FAILURE REGISTER DETERMINATION CIRCUIT
EBLOCK EXPECTED VALUE COMPARISON CIRCUIT
FAILURE BLOCK DETERMINATION CIRCUIT
BLOCK COMPRESSION UNIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
TEST PATTERN GENERATION UNIT
Tpa Tpb Tpc Tpl Tpm Tpn
17a 17b 17c 17l 17m 17n
COLLECTIVE COMPRESSION UNIT
SCAN CHAIN COMPRESSION UNIT
Dpa Dpb Dpc Dpl Dpm Dpn
DCp {DCpa, DCpb, DCpc, ... ,DCpl, DCpm, DCpn }
REGISTER INVERSION CIRCUIT
REGISTER SELECTION CIRCUIT
21
22a
23
24
25
36
5
7
32
8
9
4
3
29
18
33
34
16
2
6

FIG. 6

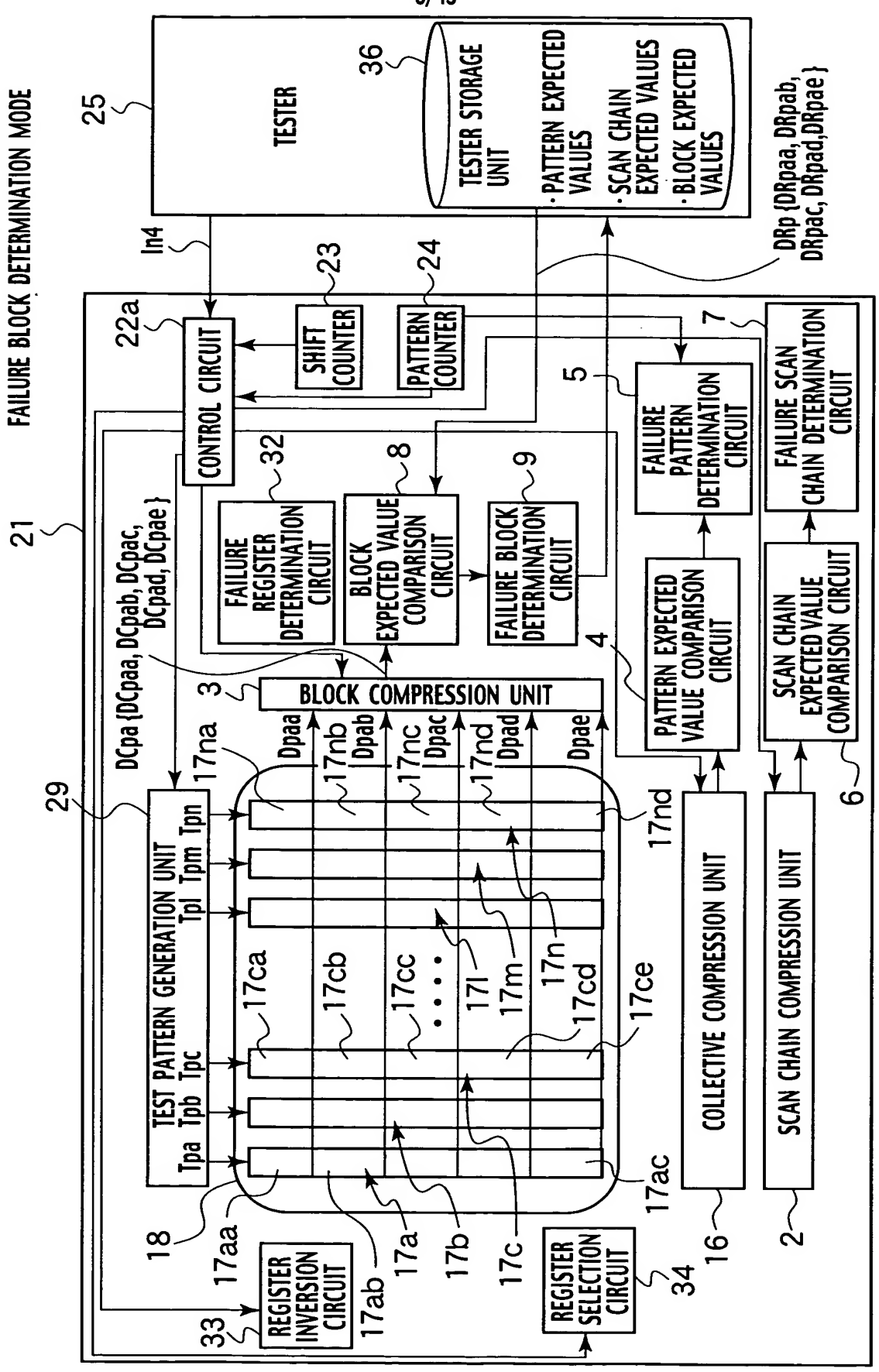

FAILURE BLOCK DETERMINATION MODE
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
DRp {DRpaa, DRpab, DRpac, DRpad, DRpae}
In4
CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
FAILURE REGISTER DETERMINATION CIRCUIT
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
FAILURE BLOCK DETERMINATION CIRCUIT
FAILURE PATTERN DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
DCpa {DCpaa, DCpab, DCpac, DCpad, DCpae}
BLOCK COMPRESSION UNIT
Dpaa
Dpab
Dpac
Dpad
Dpae
TEST PATTERN GENERATION UNIT
Tpa Tpb Tpc Tpl Tpm Tpn
COLLECTIVE COMPRESSION UNIT
SCAN CHAIN COMPRESSION UNIT
REGISTER INVERSION CIRCUIT
REGISTER SELECTION CIRCUIT
17na
17nb
17nc
17nd
17ca
17cb
17cc
17cd
17ce
17aa
17ab
17a
17b
17c
17ac
17l
17m
17n
21
22a
23
24
25
36
7
5
32
8
9
4
3
29
18
33
34
16
2
6

FIG. 7

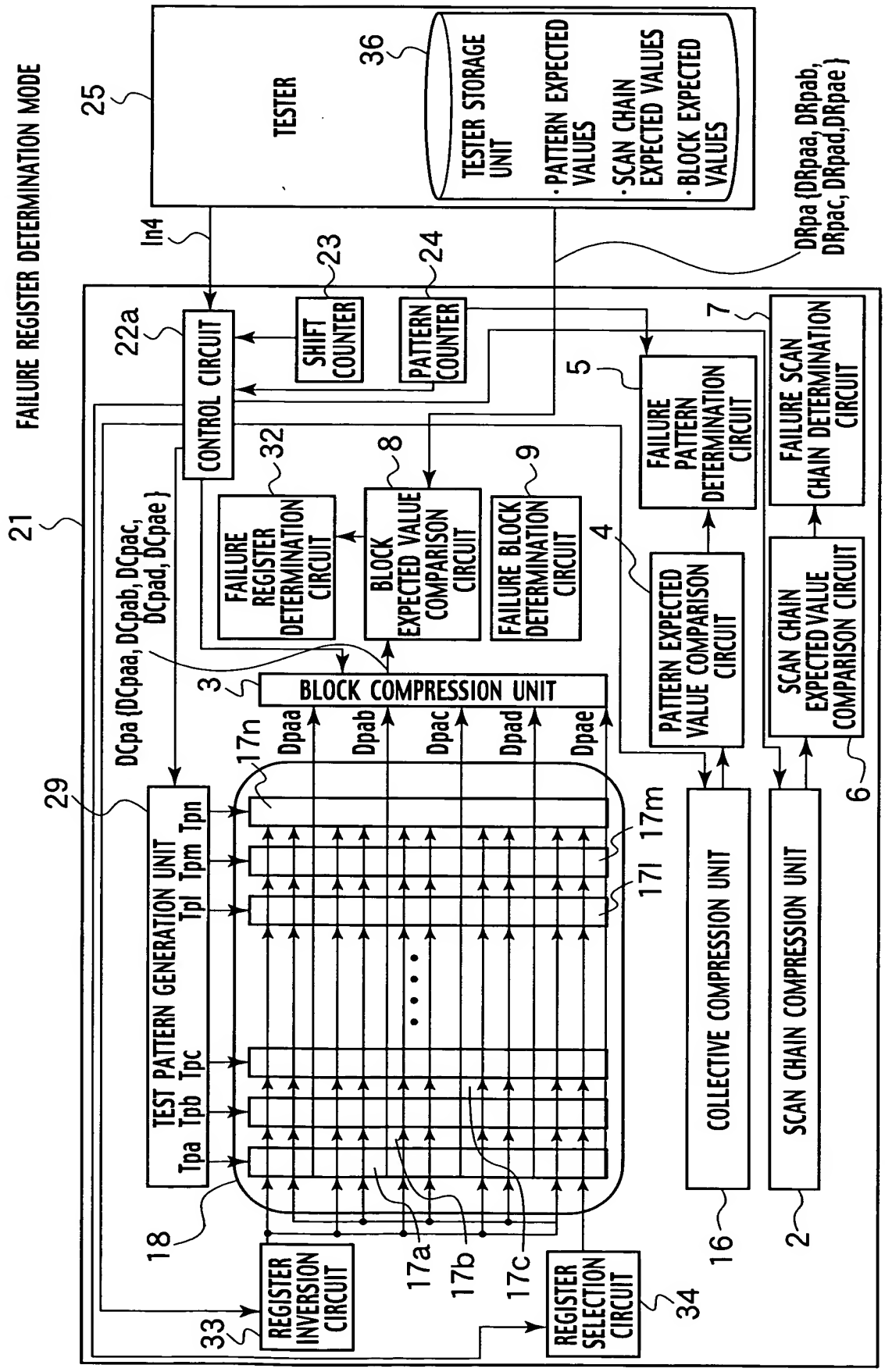

FAILURE REGISTER DETERMINATION MODE
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
DRpa {DRpaa, DRpab, DRpac, DRpad, DRpae}
In4
CONTROL CIRCUIT
SHIFT COUNTER
PATTERN COUNTER
FAILURE PATTERN DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
FAILURE REGISTER DETERMINATION CIRCUIT
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
FAILURE BLOCK DETERMINATION CIRCUIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
DCpa {DCpaa, DCpab, DCpac, DCpad, DCpae}
BLOCK COMPRESSION UNIT
Dpaa
Dpab
Dpac
Dpad
Dpae
TEST PATTERN GENERATION UNIT
Tpa Tpb Tpc Tpl Tpm Tpn
COLLECTIVE COMPRESSION UNIT
SCAN CHAIN COMPRESSION UNIT
REGISTER INVERSION CIRCUIT
REGISTER SELECTION CIRCUIT
17a
17b
17c
17l
17m
17n
2
3
4
5
6
7
8
9
16
18
21
22a
23
24
25
29
32
33
34
36

FIG. 8

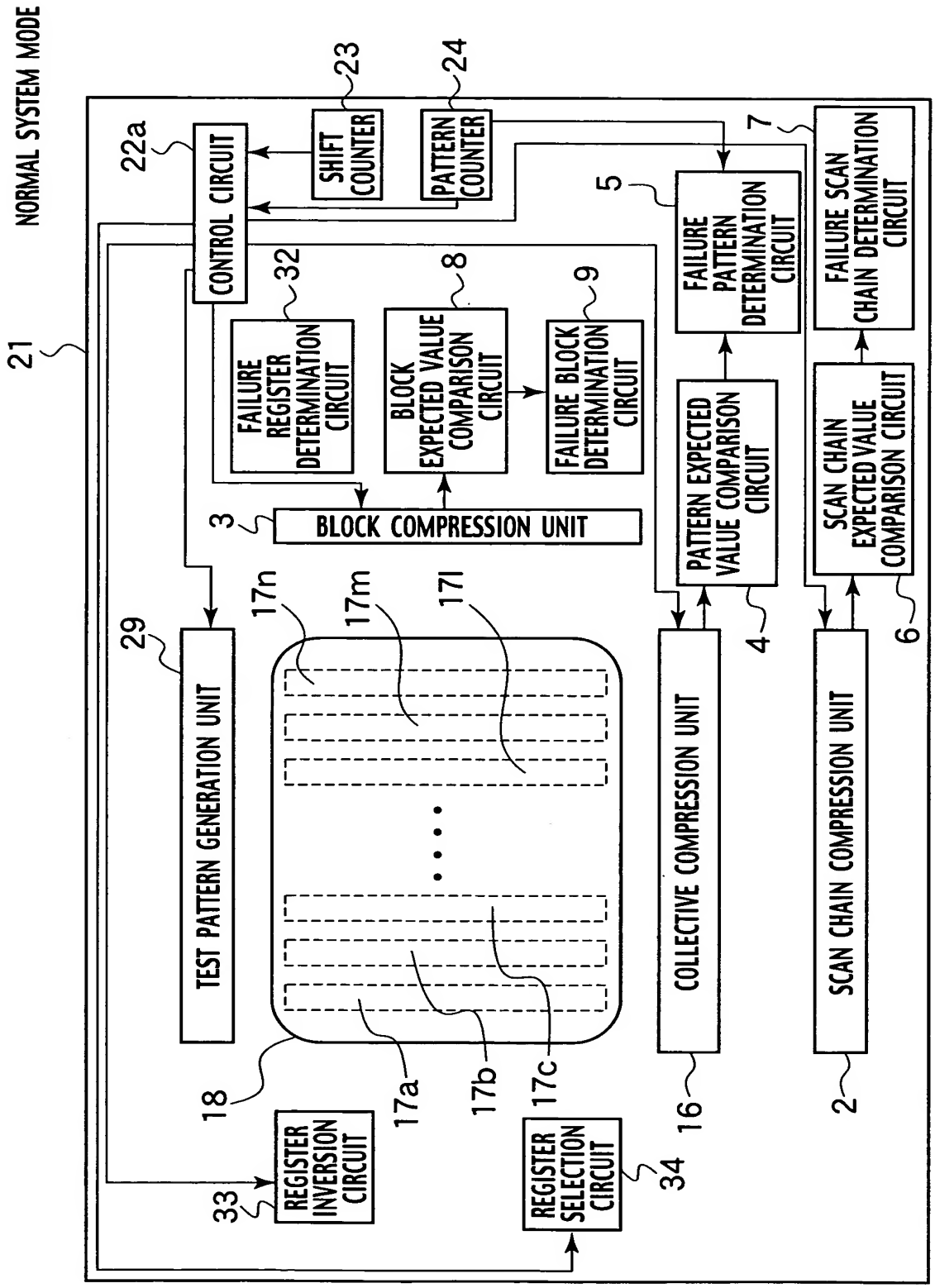

NORMAL SYSTEM MODE
21
22a
CONTROL CIRCUIT
23
SHIFT COUNTER
24
PATTERN COUNTER
7
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
5
FAILURE PATTERN DETERMINATION CIRCUIT
32
FAILURE REGISTER DETERMINATION CIRCUIT
8
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
9
FAILURE BLOCK DETERMINATION CIRCUIT
3
BLOCK COMPRESSION UNIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
29
TEST PATTERN GENERATION UNIT
17n
17m
17l
COLLECTIVE COMPRESSION UNIT
SCAN CHAIN COMPRESSION UNIT
4
6
18
17a
17b
17c
16
2
33
REGISTER INVERSION CIRCUIT
REGISTER SELECTION CIRCUIT
34

FIG. 9

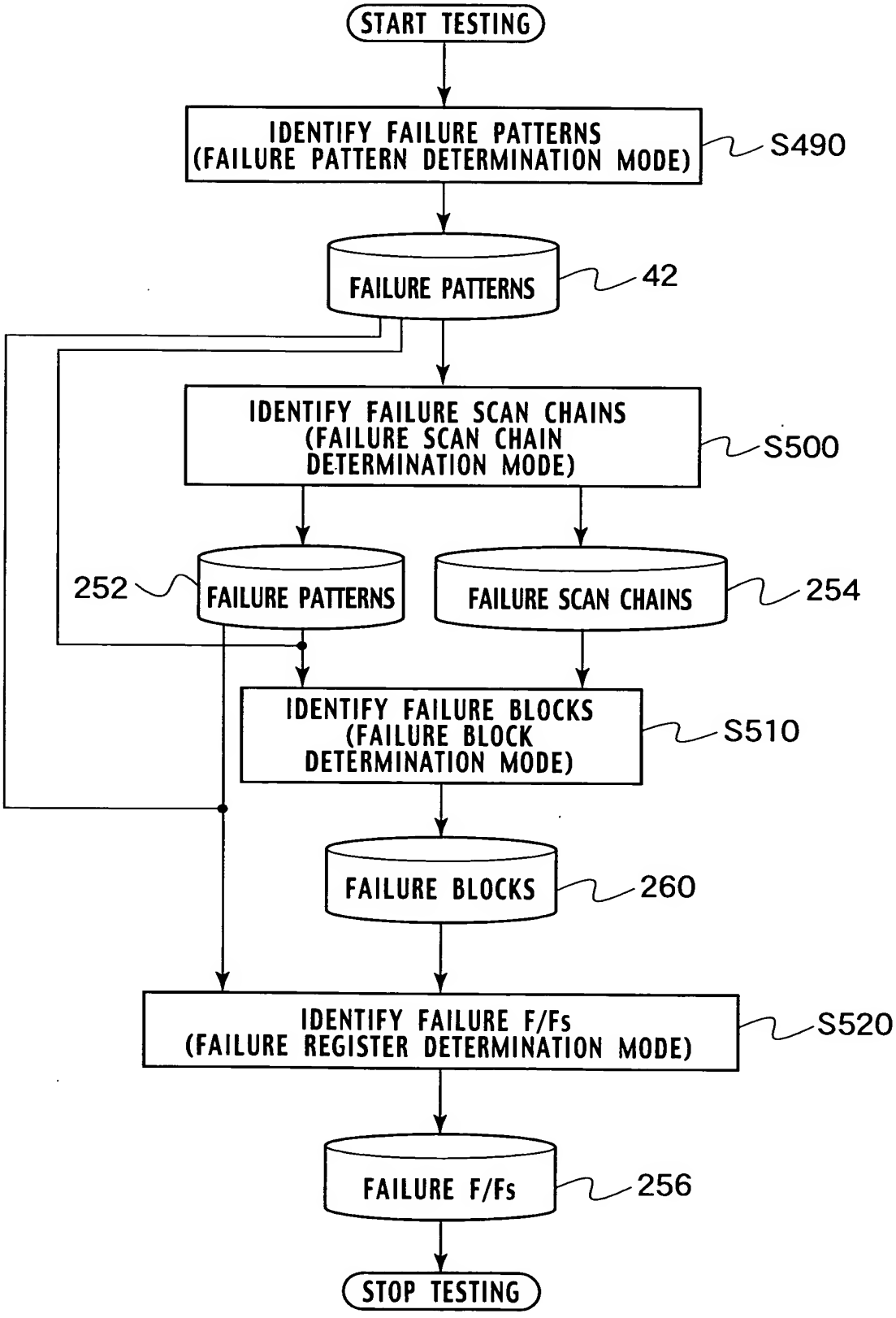

START TESTING
IDENTIFY FAILURE PATTERNS (FAILURE PATTERN DETERMINATION MODE)
S490
FAILURE PATTERNS
42
IDENTIFY FAILURE SCAN CHAINS (FAILURE SCAN CHAIN DETERMINATION MODE)
S500
252
FAILURE PATTERNS
FAILURE SCAN CHAINS
254
IDENTIFY FAILURE BLOCKS (FAILURE BLOCK DETERMINATION MODE)
S510
FAILURE BLOCKS
260
IDENTIFY FAILURE F/Fs (FAILURE REGISTER DETERMINATION MODE)
S520
FAILURE F/Fs
256
STOP TESTING

FIG. 10

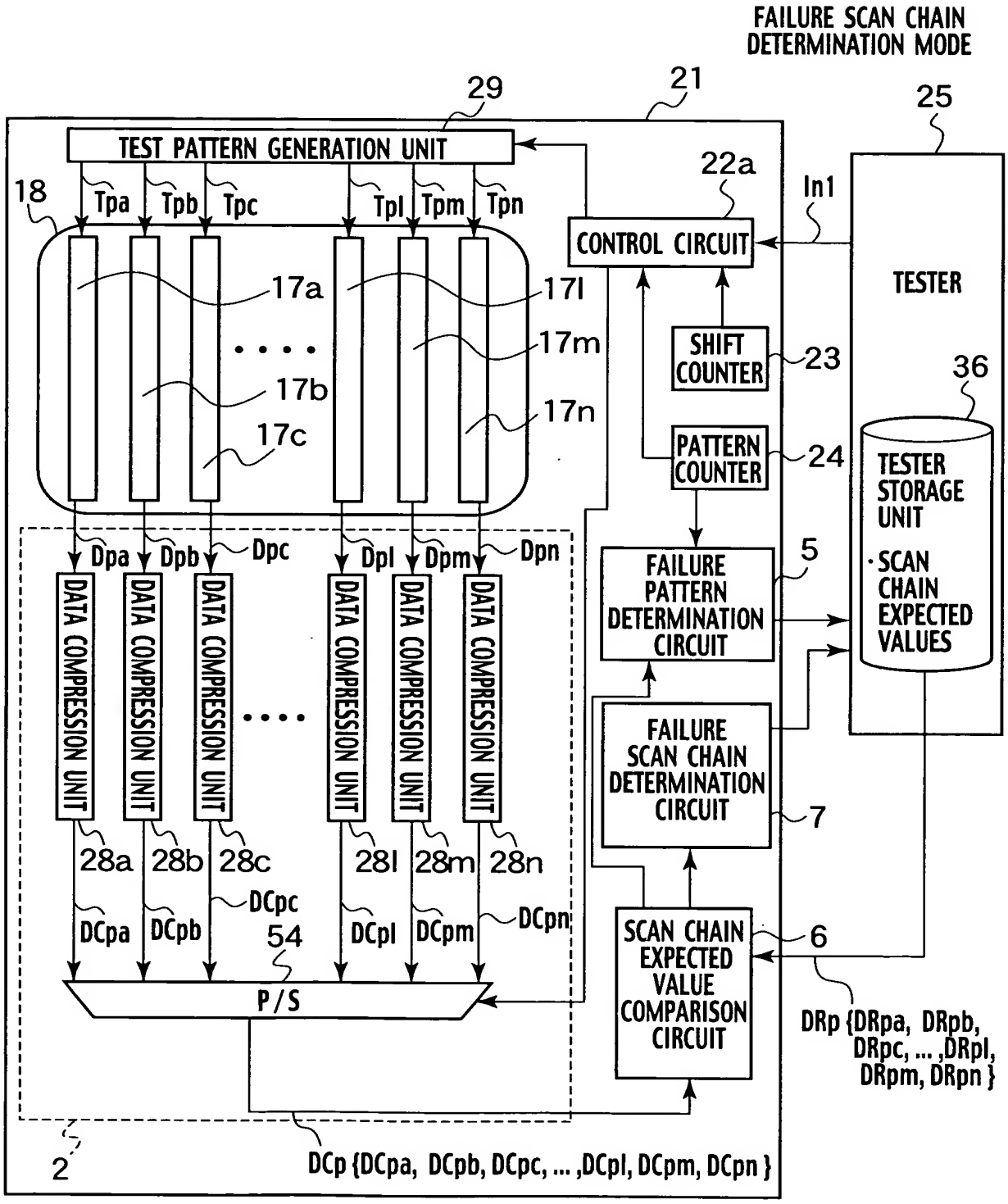

FAILURE SCAN CHAIN DETERMINATION MODE
29
21
25
TEST PATTERN GENERATION UNIT
22a
In1
18
Tpa
Tpb
Tpc
Tpl
Tpm
Tpn
CONTROL CIRCUIT
TESTER
17a
17l
17m
17b
17n
17c
SHIFT COUNTER
23
36
PATTERN COUNTER
24
TESTER STORAGE UNIT
· SCAN CHAIN EXPECTED VALUES
Dpa
Dpb
Dpc
Dpl
Dpm
Dpn
FAILURE PATTERN DETERMINATION CIRCUIT
5
DATA COMPRESSION UNIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
7
28a
28b
28c
28l
28m
28n
DCpc
DCpa
DCpb
54
DCpl
DCpm
DCpn
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
6
P/S
DRp {DRpa, DRpb, DRpc, ... ,DRpl, DRpm, DRpn }
2
DCp {DCpa, DCpb, DCpc, ... ,DCpl, DCpm, DCpn }

FIG. 11

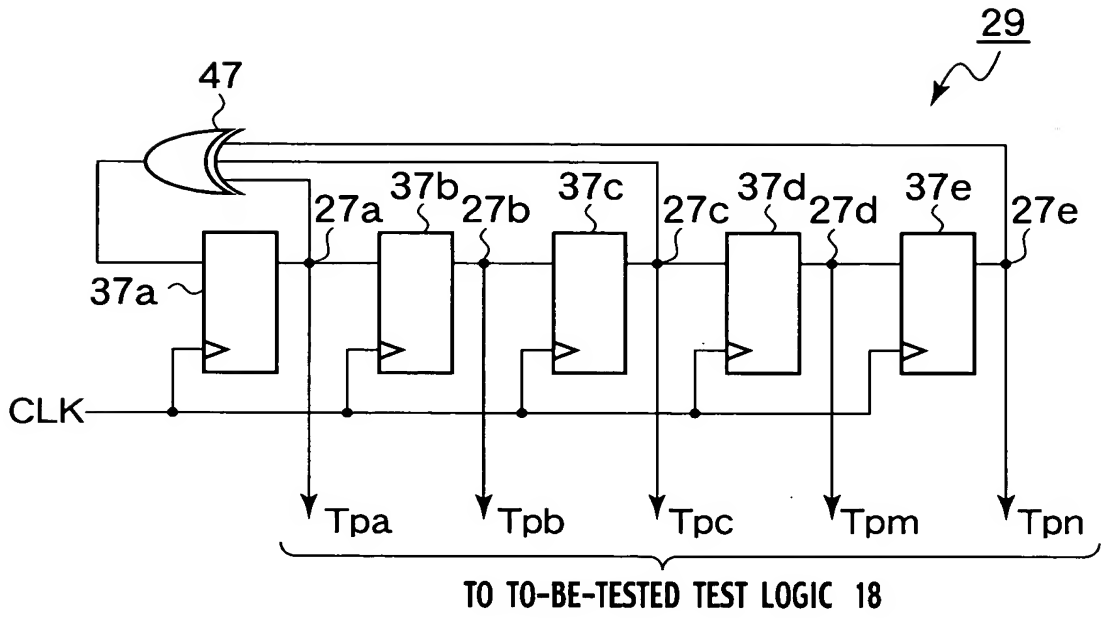

29
47
27a
37b
27b
37c
27c
37d
27d
37e
27e
37a
CLK
Tpa
Tpb
Tpc
Tpm
Tpn
TO TO-BE-TESTED TEST LOGIC 18

FIG. 12

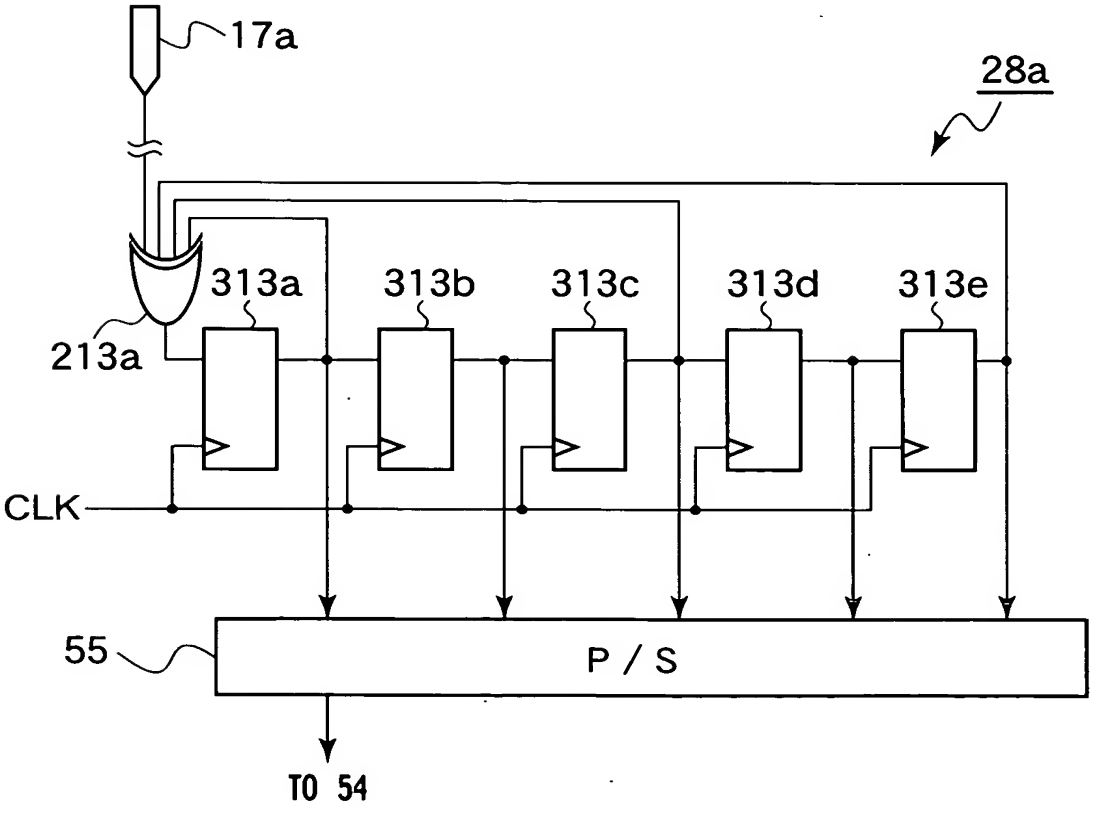

17a
28a
313a
313b
313c
313d
313e
213a
CLK
55
P / S
TO 54

FIG. 13

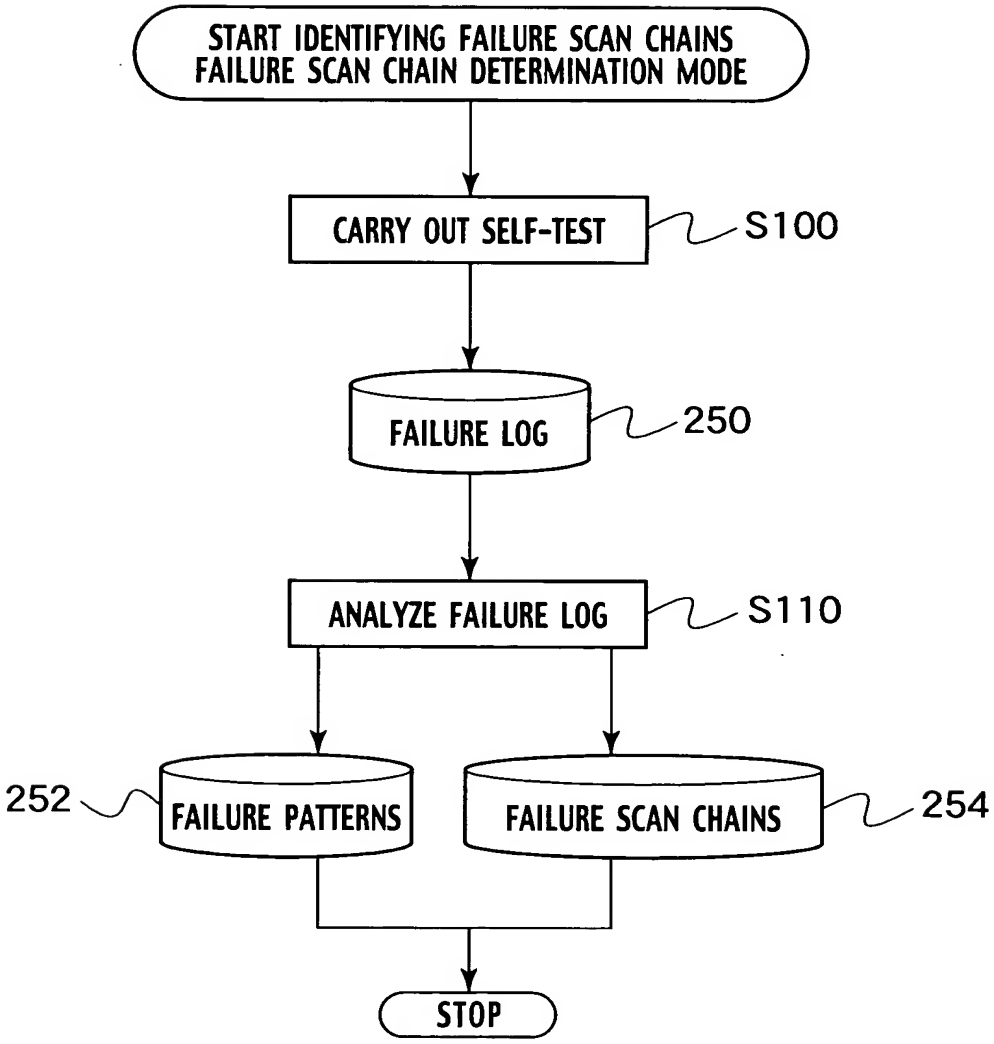

START IDENTIFYING FAILURE SCAN CHAINS
FAILURE SCAN CHAIN DETERMINATION MODE
CARRY OUT SELF-TEST
S100
FAILURE LOG
250
ANALYZE FAILURE LOG
S110
252
FAILURE PATTERNS
FAILURE SCAN CHAINS
254
STOP

FIG. 14

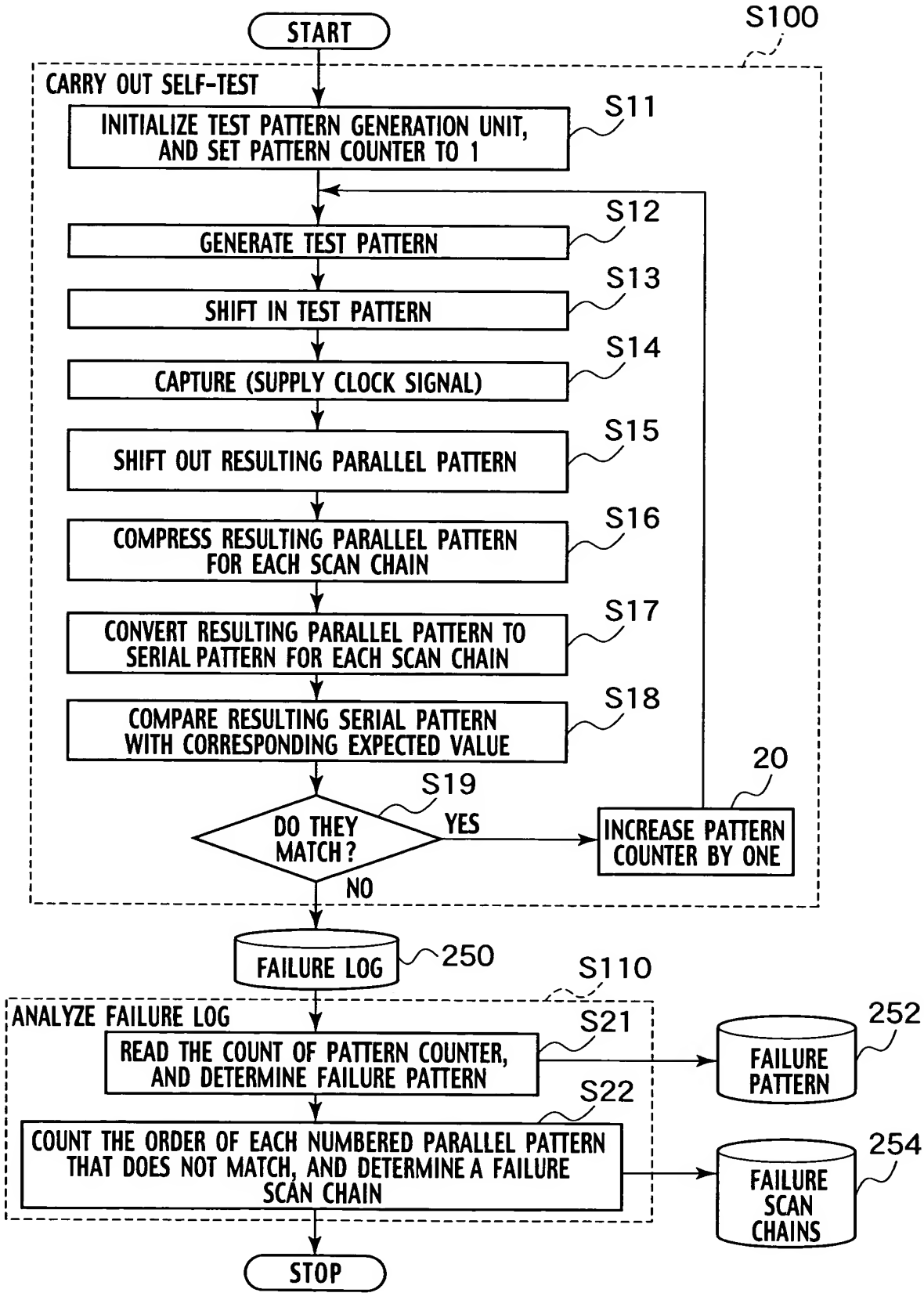

START
S100
CARRY OUT SELF-TEST
INITIALIZE TEST PATTERN GENERATION UNIT, AND SET PATTERN COUNTER TO 1
S11
GENERATE TEST PATTERN
S12
SHIFT IN TEST PATTERN
S13
CAPTURE (SUPPLY CLOCK SIGNAL)
S14
SHIFT OUT RESULTING PARALLEL PATTERN
S15
COMPRESS RESULTING PARALLEL PATTERN FOR EACH SCAN CHAIN
S16
CONVERT RESULTING PARALLEL PATTERN TO SERIAL PATTERN FOR EACH SCAN CHAIN
S17
COMPARE RESULTING SERIAL PATTERN WITH CORRESPONDING EXPECTED VALUE
S18
S19
DO THEY MATCH?
YES
NO
20
INCREASE PATTERN COUNTER BY ONE
FAILURE LOG
250
S110
ANALYZE FAILURE LOG
READ THE COUNT OF PATTERN COUNTER, AND DETERMINE FAILURE PATTERN
S21
252
FAILURE PATTERN
S22
COUNT THE ORDER OF EACH NUMBERED PARALLEL PATTERN THAT DOES NOT MATCH, AND DETERMINE A FAILURE SCAN CHAIN
254
FAILURE SCAN CHAINS
STOP

FIG. 15

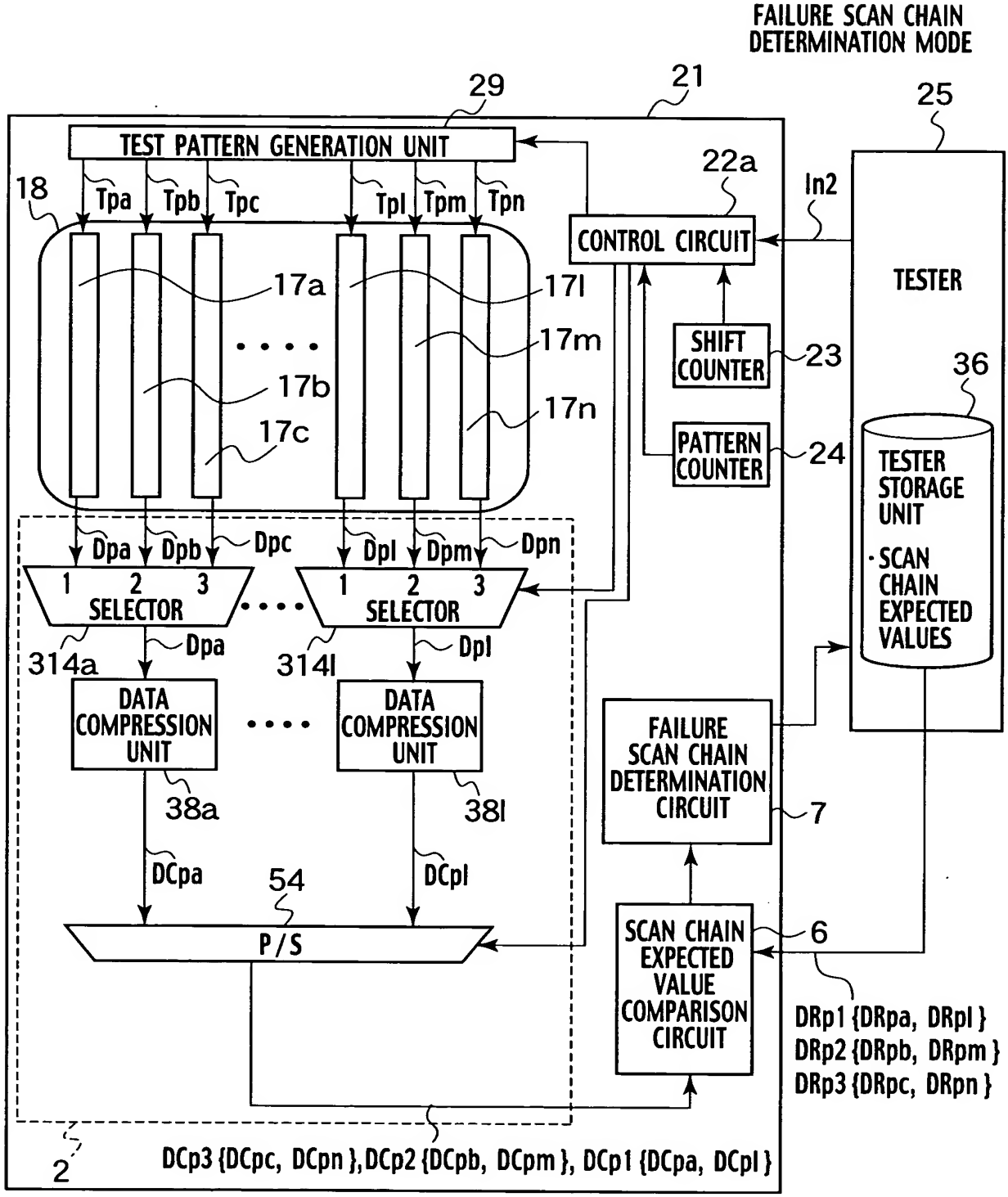

FAILURE SCAN CHAIN DETERMINATION MODE
29
21
25
TEST PATTERN GENERATION UNIT
22a
18
Tpa
Tpb
Tpc
Tpl
Tpm
Tpn
In2
CONTROL CIRCUIT
TESTER
17a
17l
17m
17b
17n
17c
SHIFT COUNTER
23
36
PATTERN COUNTER
24
TESTER STORAGE UNIT
· SCAN CHAIN EXPECTED VALUES
Dpa
Dpb
Dpc
Dpl
Dpm
Dpn
1 2 3
SELECTOR
1 2 3
SELECTOR
314a
314l
Dpa
Dpl
DATA COMPRESSION UNIT
DATA COMPRESSION UNIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
7
38a
38l
DCpa
54
DCpl
P/S
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
6
DRp1 {DRpa, DRpl }
DRp2 {DRpb, DRpm }
DRp3 {DRpc, DRpn }
2
DCp3 {DCpc, DCpn }, DCp2 {DCpb, DCpm }, DCp1 {DCpa, DCpl }

FIG. 16

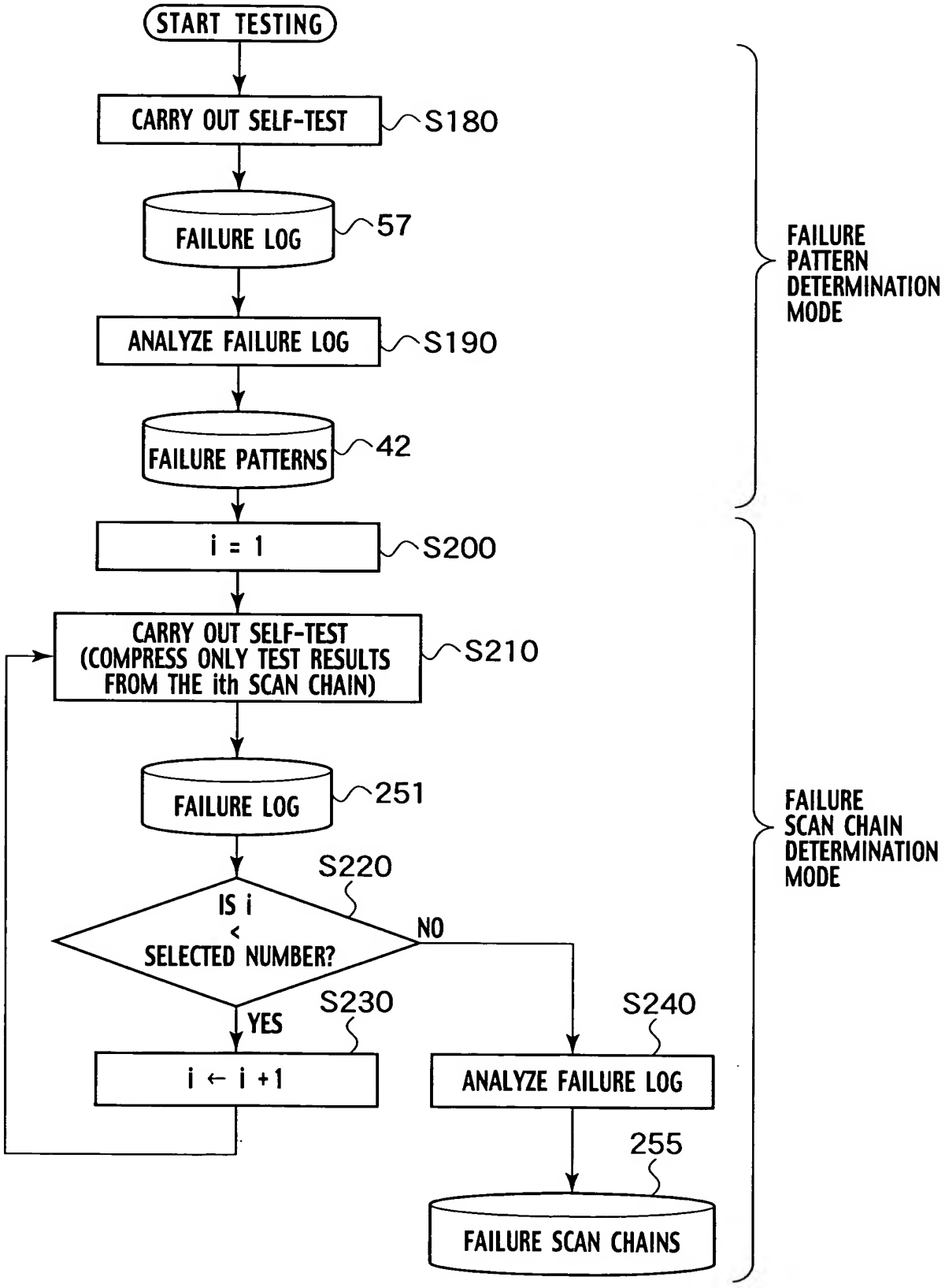

START TESTING
CARRY OUT SELF-TEST
S180
FAILURE LOG
57
ANALYZE FAILURE LOG
S190
FAILURE PATTERNS
42
FAILURE PATTERN DETERMINATION MODE
i = 1
S200
CARRY OUT SELF-TEST (COMPRESS ONLY TEST RESULTS FROM THE ith SCAN CHAIN)
S210
FAILURE LOG
251
S220
IS i < SELECTED NUMBER?
NO
YES
S230
i ← i +1
S240
ANALYZE FAILURE LOG
255
FAILURE SCAN CHAINS
FAILURE SCAN CHAIN DETERMINATION MODE

FIG. 17

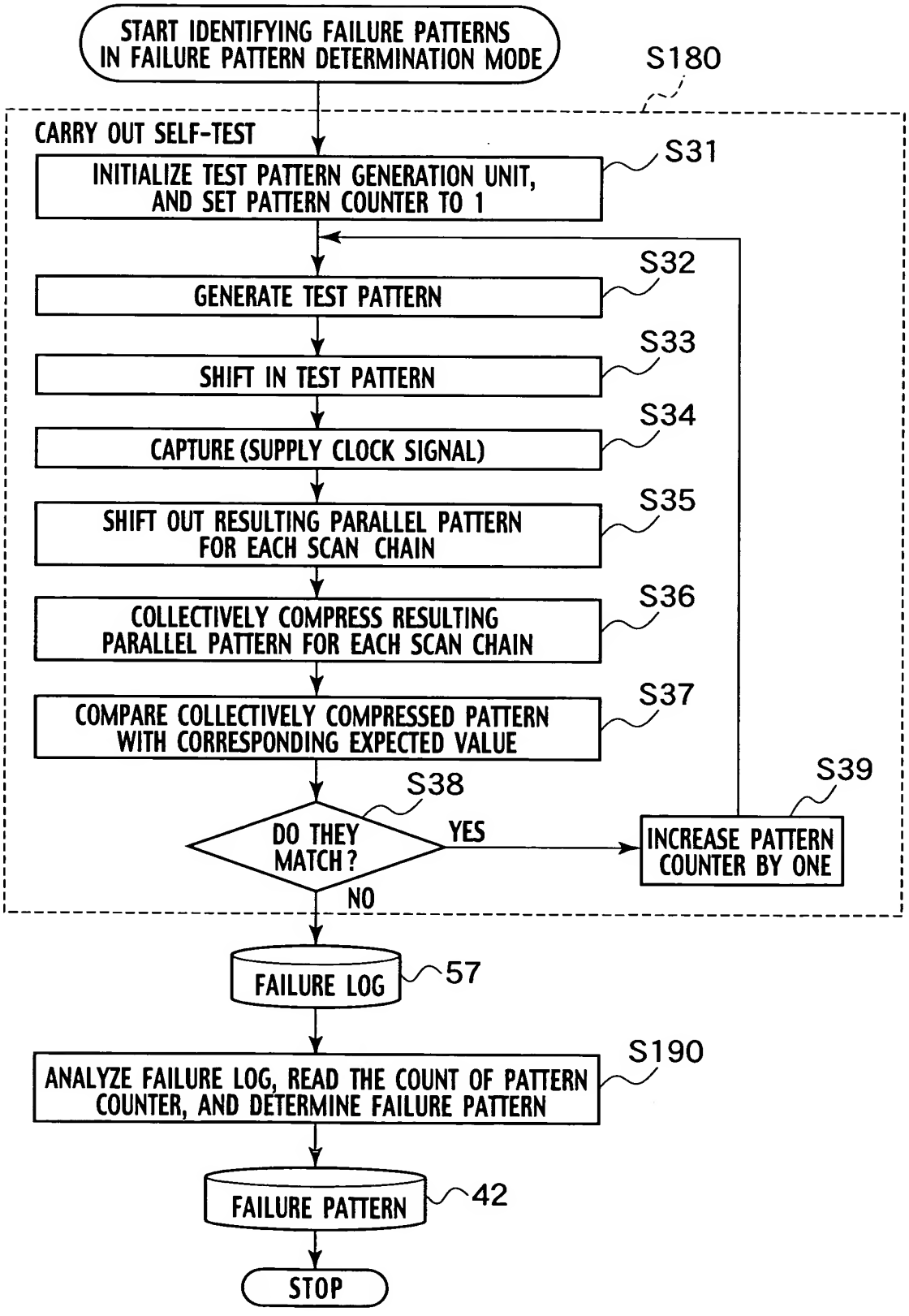

START IDENTIFYING FAILURE PATTERNS IN FAILURE PATTERN DETERMINATION MODE
S180
CARRY OUT SELF-TEST
INITIALIZE TEST PATTERN GENERATION UNIT, AND SET PATTERN COUNTER TO 1
S31
GENERATE TEST PATTERN
S32
SHIFT IN TEST PATTERN
S33
CAPTURE (SUPPLY CLOCK SIGNAL)
S34
SHIFT OUT RESULTING PARALLEL PATTERN FOR EACH SCAN CHAIN
S35
COLLECTIVELY COMPRESS RESULTING PARALLEL PATTERN FOR EACH SCAN CHAIN
S36
COMPARE COLLECTIVELY COMPRESSED PATTERN WITH CORRESPONDING EXPECTED VALUE
S37
S38
DO THEY MATCH?
YES
S39
INCREASE PATTERN COUNTER BY ONE
NO
FAILURE LOG
57
S190
ANALYZE FAILURE LOG, READ THE COUNT OF PATTERN COUNTER, AND DETERMINE FAILURE PATTERN
FAILURE PATTERN
42
STOP

FIG. 18

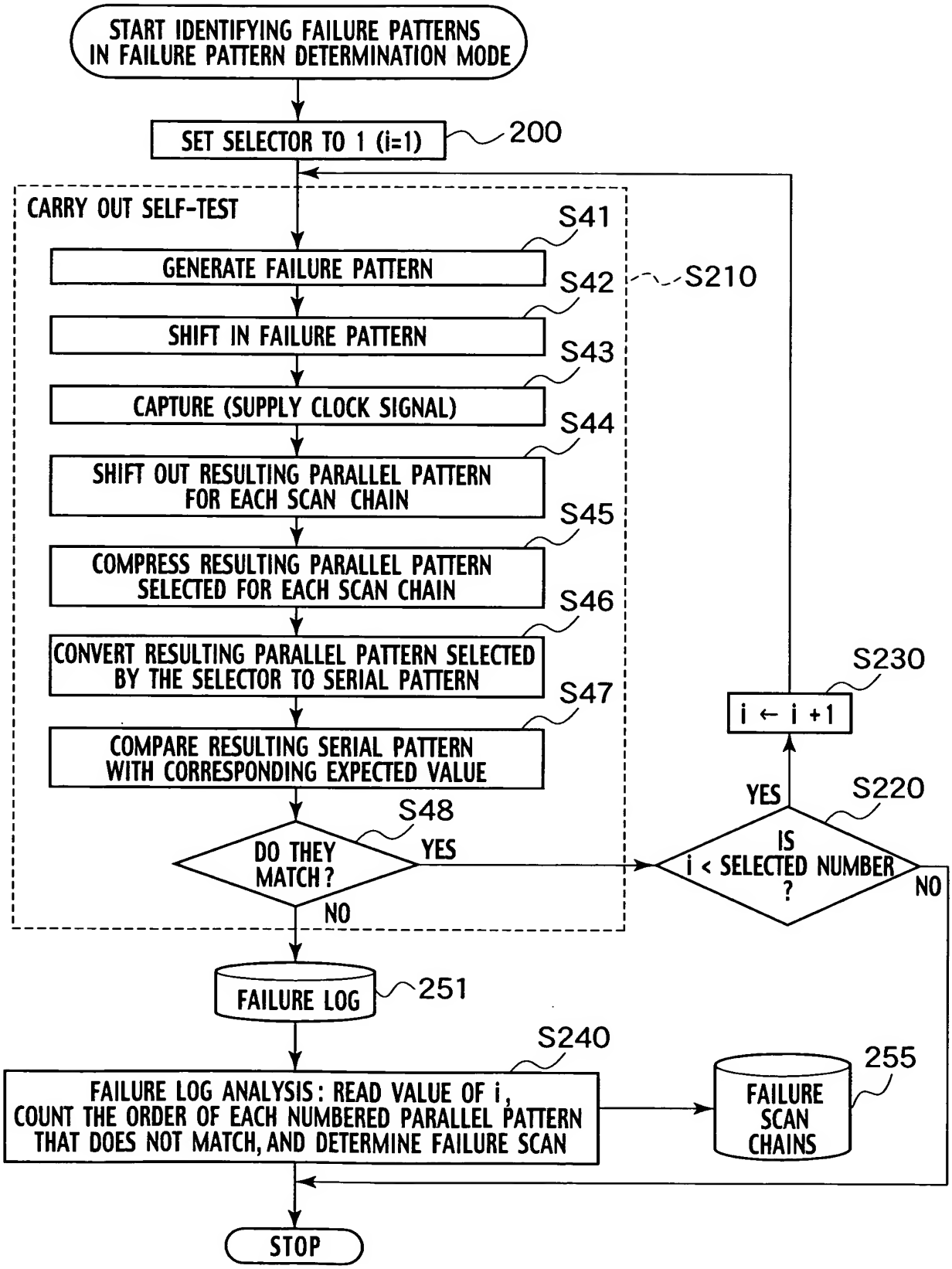

START IDENTIFYING FAILURE PATTERNS IN FAILURE PATTERN DETERMINATION MODE
SET SELECTOR TO 1 (i=1)
200
CARRY OUT SELF-TEST
S41
GENERATE FAILURE PATTERN
S42
SHIFT IN FAILURE PATTERN
S43
CAPTURE (SUPPLY CLOCK SIGNAL)
S44
SHIFT OUT RESULTING PARALLEL PATTERN FOR EACH SCAN CHAIN
S45
COMPRESS RESULTING PARALLEL PATTERN SELECTED FOR EACH SCAN CHAIN
S46
CONVERT RESULTING PARALLEL PATTERN SELECTED BY THE SELECTOR TO SERIAL PATTERN
S47
COMPARE RESULTING SERIAL PATTERN WITH CORRESPONDING EXPECTED VALUE
S48
DO THEY MATCH?
YES
NO
S210
S220
IS i < SELECTED NUMBER ?
YES
NO
S230
i ← i +1
FAILURE LOG
251
S240
FAILURE LOG ANALYSIS: READ VALUE OF i, COUNT THE ORDER OF EACH NUMBERED PARALLEL PATTERN THAT DOES NOT MATCH, AND DETERMINE FAILURE SCAN
255
FAILURE SCAN CHAINS
STOP

FIG. 19

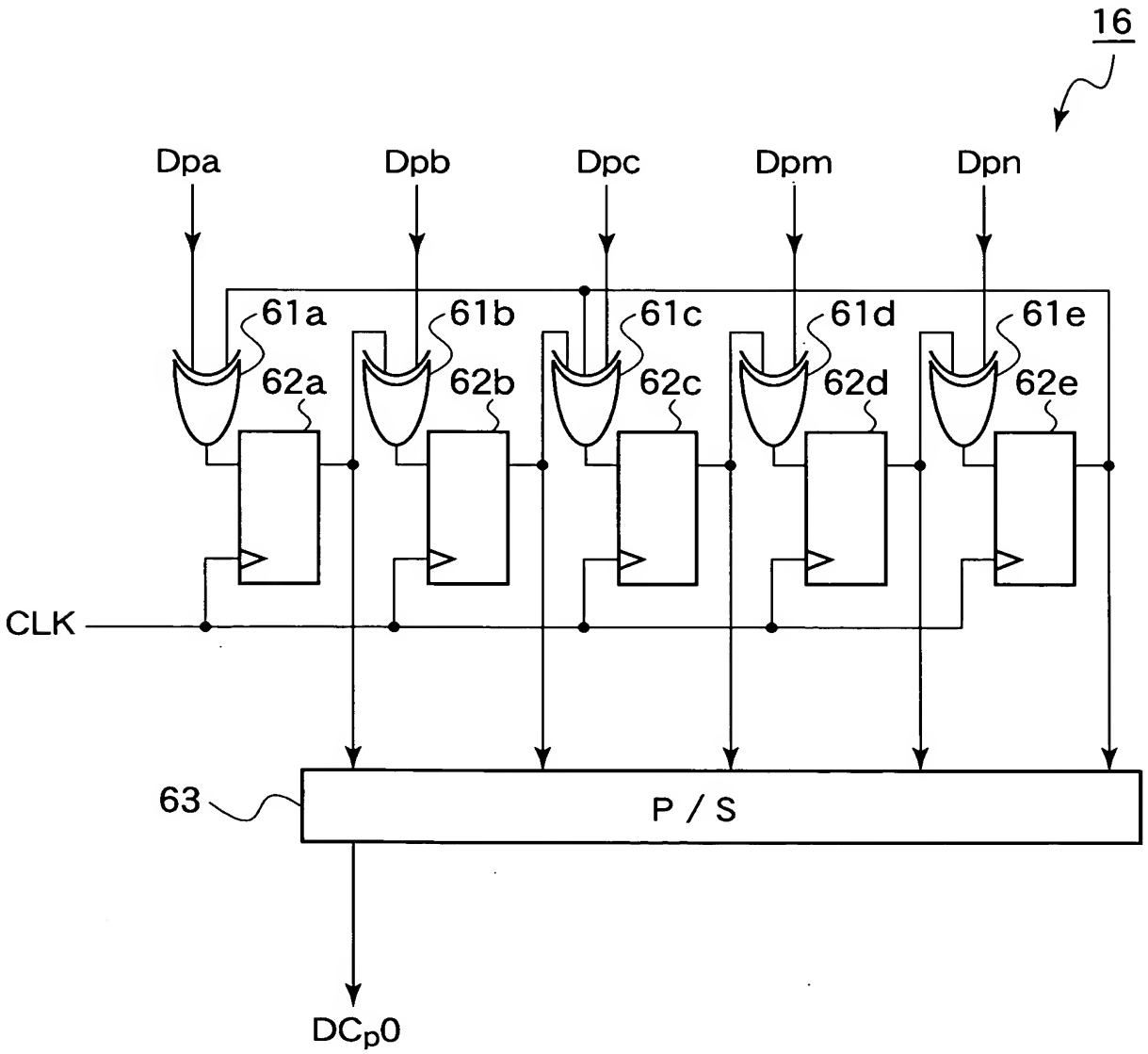

16
Dpa
Dpb
Dpc
Dpm
Dpn
61a
61b
61c
61d
61e
62a
62b
62c
62d
62e
CLK
63
P / S
DCp0

FIG. 20

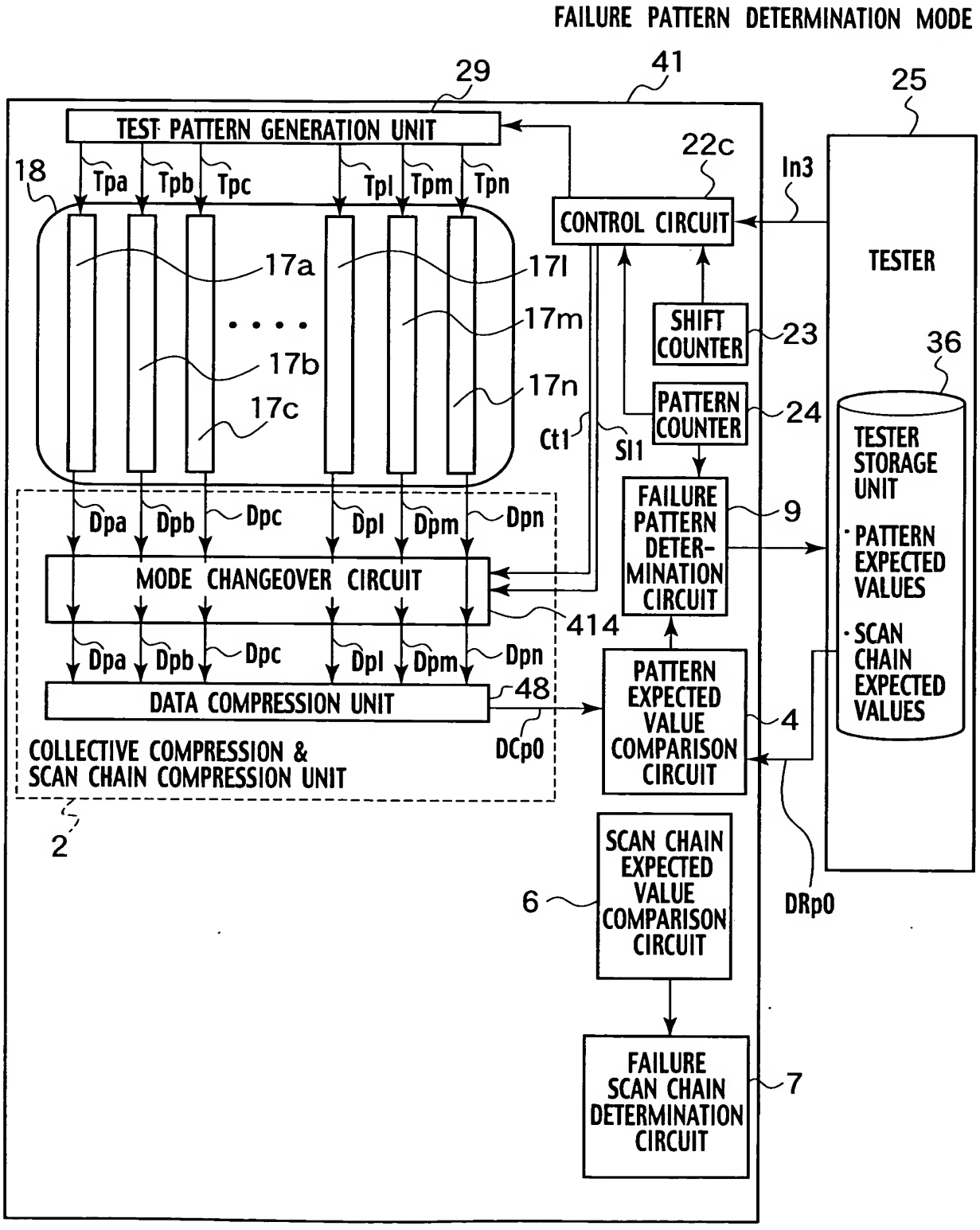

FAILURE PATTERN DETERMINATION MODE
29
41
25
TEST PATTERN GENERATION UNIT
22c
18
Tpa
Tpb
Tpc
Tpl
Tpm
Tpn
In3
CONTROL CIRCUIT
TESTER
17a
17l
17m
17b
17n
17c
SHIFT COUNTER
23
36
PATTERN COUNTER
24
Ct1
Sl1
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
FAILURE PATTERN DETER-MINATION CIRCUIT
9
Dpa
Dpb
Dpc
Dpl
Dpm
Dpn
MODE CHANGEOVER CIRCUIT
414
DATA COMPRESSION UNIT
48
DCp0
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
4
COLLECTIVE COMPRESSION & SCAN CHAIN COMPRESSION UNIT
2
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
6
DRp0
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
7

FIG. 21

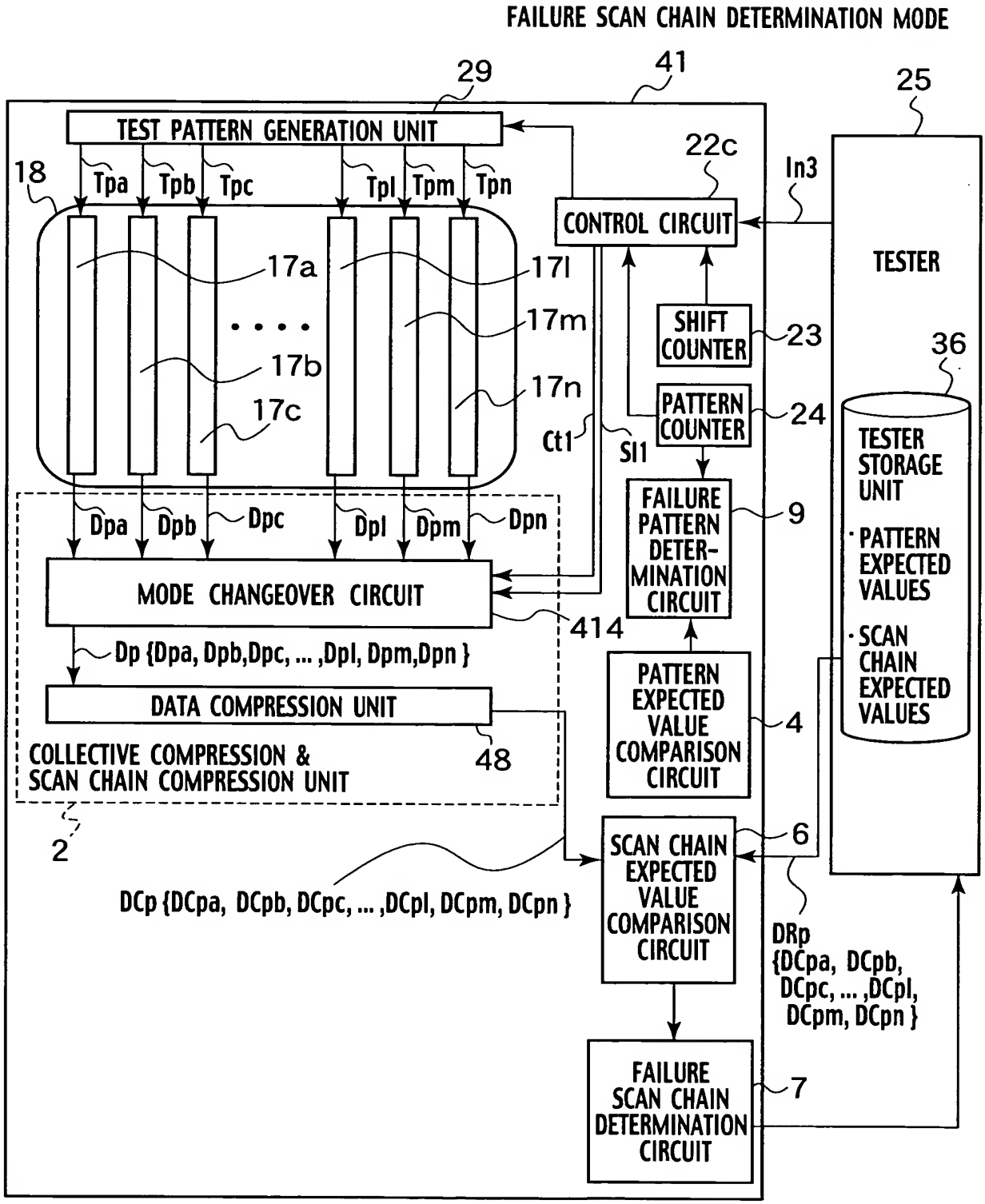

FAILURE SCAN CHAIN DETERMINATION MODE
29
41
25
TEST PATTERN GENERATION UNIT
22c
In3
18
Tpa
Tpb
Tpc
Tpl
Tpm
Tpn
CONTROL CIRCUIT
TESTER
17a
17l
17m
17b
17n
17c
SHIFT COUNTER
23
36
PATTERN COUNTER
24
Ct1
Sl1
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
FAILURE PATTERN DETER-MINATION CIRCUIT
9
Dpa
Dpb
Dpc
Dpl
Dpm
Dpn
MODE CHANGEOVER CIRCUIT
414
Dp {Dpa, Dpb,Dpc, ... ,Dpl, Dpm,Dpn }
DATA COMPRESSION UNIT
48
COLLECTIVE COMPRESSION & SCAN CHAIN COMPRESSION UNIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
4
2
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
6
DCp {DCpa, DCpb, DCpc, ... ,DCpl, DCpm, DCpn }
DRp {DCpa, DCpb, DCpc, ... ,DCpl, DCpm, DCpn }
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
7

FIG. 22

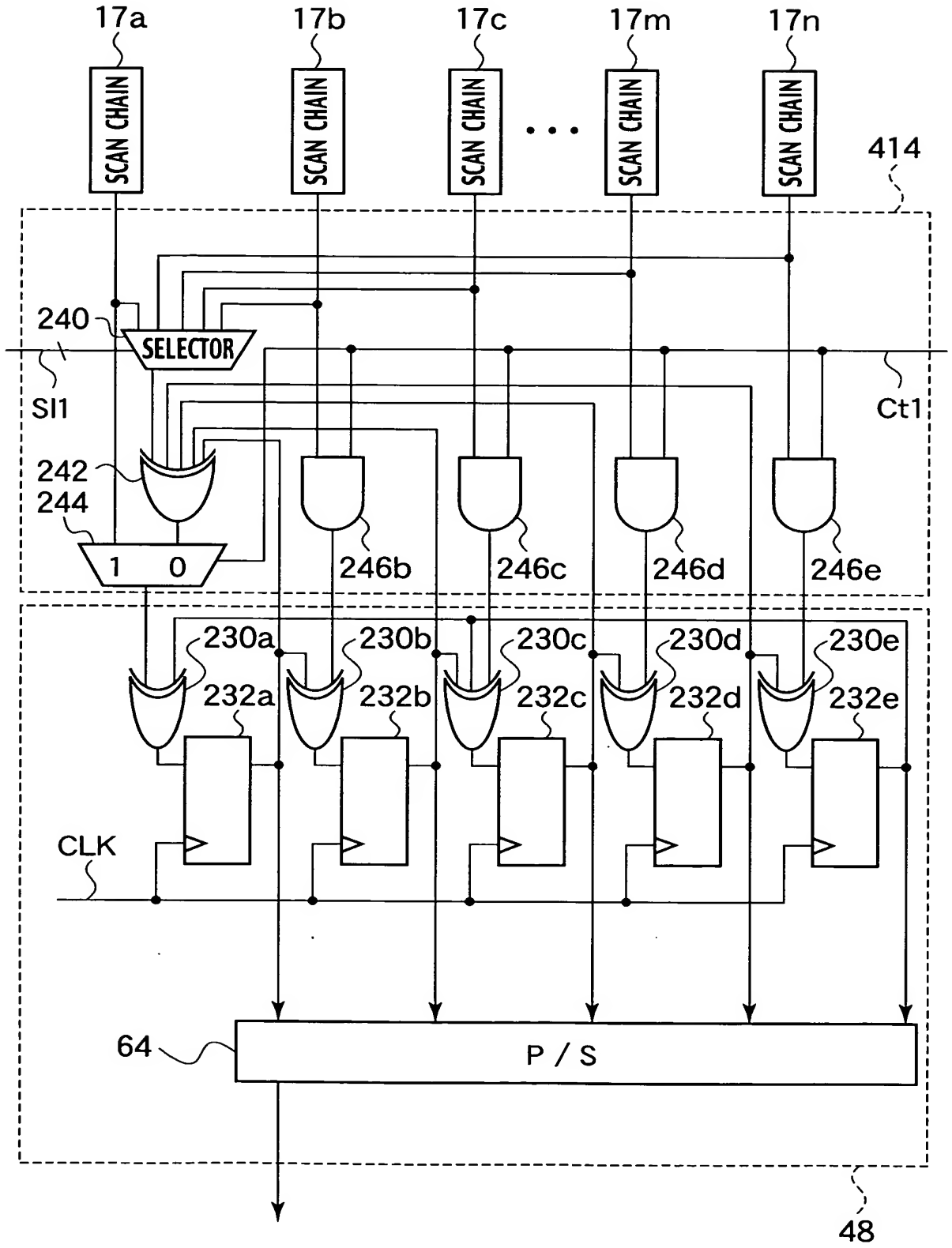

17a
17b
17c
17m
17n
SCAN CHAIN
SCAN CHAIN
SCAN CHAIN
SCAN CHAIN
SCAN CHAIN
414
240
SELECTOR
SI1
Ct1
242
244
1 0
246b
246c
246d
246e
230a
230b
230c
230d
230e
232a
232b
232c
232d
232e
CLK
64
P / S
48

FIG. 23

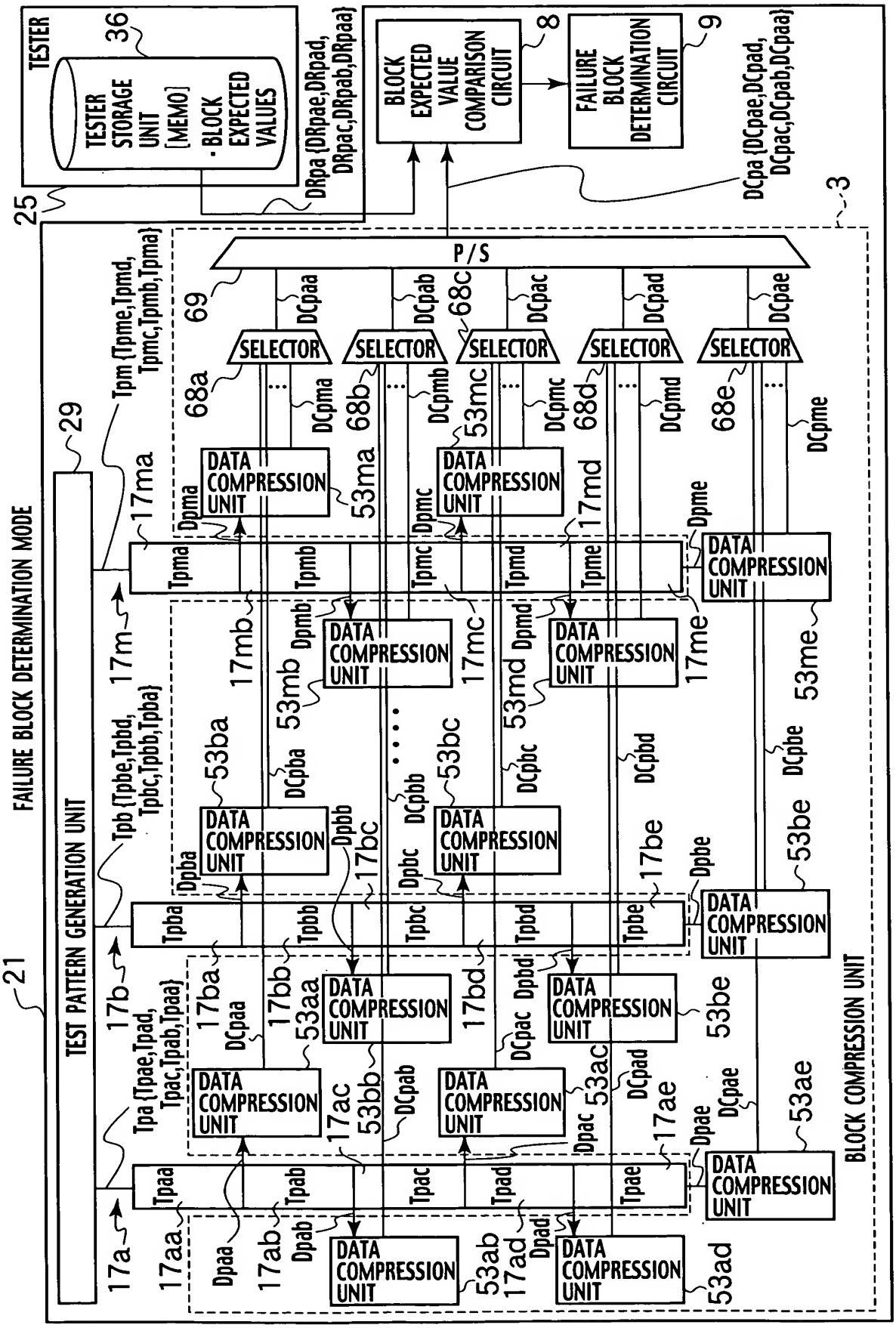

TESTER
TESTER STORAGE UNIT [MEMO]
· BLOCK EXPECTED VALUES
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
FAILURE BLOCK DETERMINATION CIRCUIT
DRpa {DRpae,DRpad, DRpac,DRpab,DRpaa}
DCpa {DCpae,DCpad, DCpac,DCpab,DCpaa}
FAILURE BLOCK DETERMINATION MODE
TEST PATTERN GENERATION UNIT
BLOCK COMPRESSION UNIT
P/S
SELECTOR
DATA COMPRESSION UNIT
Tpm {Tpme,Tpmd, Tpmc,Tpmb,Tpma}
Tpb {Tpbe,Tpbd, Tpbc,Tpbb,Tpba}
Tpa {Tpae,Tpad, Tpac,Tpab,Tpaa}

FIG. 24

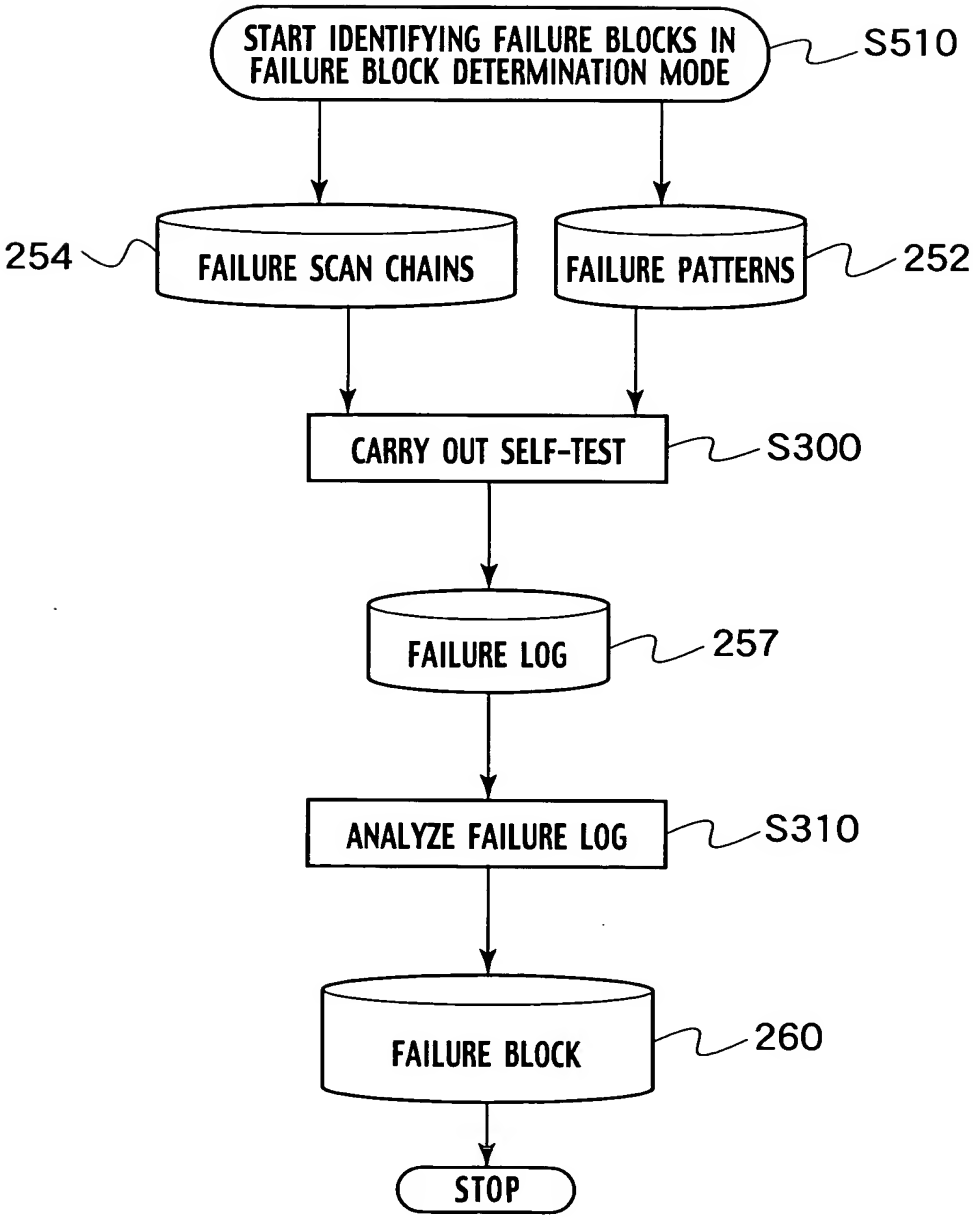

START IDENTIFYING FAILURE BLOCKS IN FAILURE BLOCK DETERMINATION MODE
S510
254
FAILURE SCAN CHAINS
FAILURE PATTERNS
252
CARRY OUT SELF-TEST
S300
FAILURE LOG
257
ANALYZE FAILURE LOG
S310
FAILURE BLOCK
260
STOP

FIG. 25

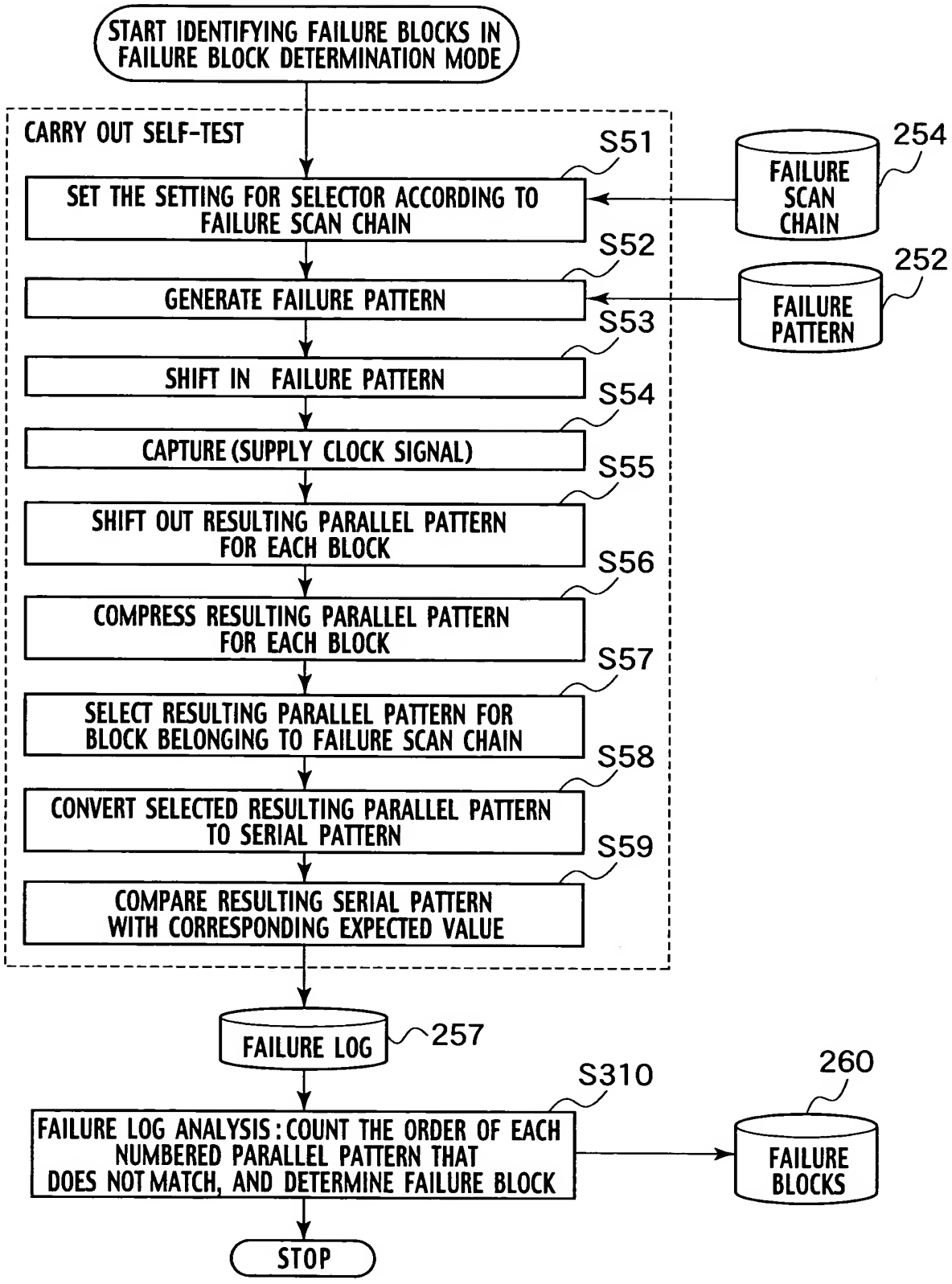

START IDENTIFYING FAILURE BLOCKS IN FAILURE BLOCK DETERMINATION MODE
CARRY OUT SELF-TEST
S51
SET THE SETTING FOR SELECTOR ACCORDING TO FAILURE SCAN CHAIN
254
FAILURE SCAN CHAIN
S52
GENERATE FAILURE PATTERN
252
FAILURE PATTERN
S53
SHIFT IN FAILURE PATTERN
S54
CAPTURE (SUPPLY CLOCK SIGNAL)
S55
SHIFT OUT RESULTING PARALLEL PATTERN FOR EACH BLOCK
S56
COMPRESS RESULTING PARALLEL PATTERN FOR EACH BLOCK
S57
SELECT RESULTING PARALLEL PATTERN FOR BLOCK BELONGING TO FAILURE SCAN CHAIN
S58
CONVERT SELECTED RESULTING PARALLEL PATTERN TO SERIAL PATTERN
S59
COMPARE RESULTING SERIAL PATTERN WITH CORRESPONDING EXPECTED VALUE
FAILURE LOG
257
S310
FAILURE LOG ANALYSIS : COUNT THE ORDER OF EACH NUMBERED PARALLEL PATTERN THAT DOES NOT MATCH, AND DETERMINE FAILURE BLOCK
260
FAILURE BLOCKS
STOP

FIG. 26

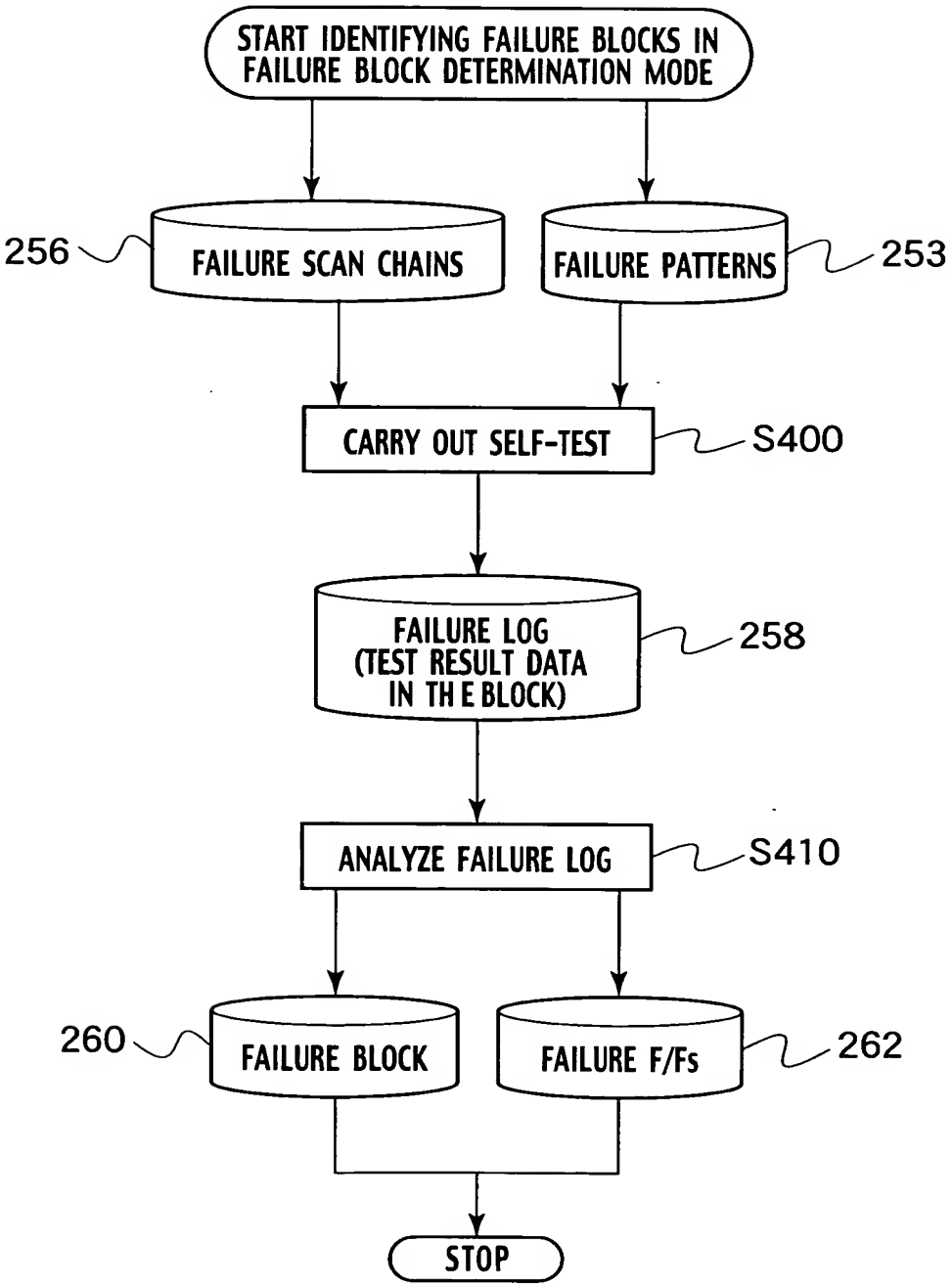

START IDENTIFYING FAILURE BLOCKS IN FAILURE BLOCK DETERMINATION MODE
256
FAILURE SCAN CHAINS
FAILURE PATTERNS
253
CARRY OUT SELF-TEST
S400
FAILURE LOG (TEST RESULT DATA IN TH E BLOCK)
258
ANALYZE FAILURE LOG
S410
260
FAILURE BLOCK
FAILURE F/Fs
262
STOP

FIG. 27

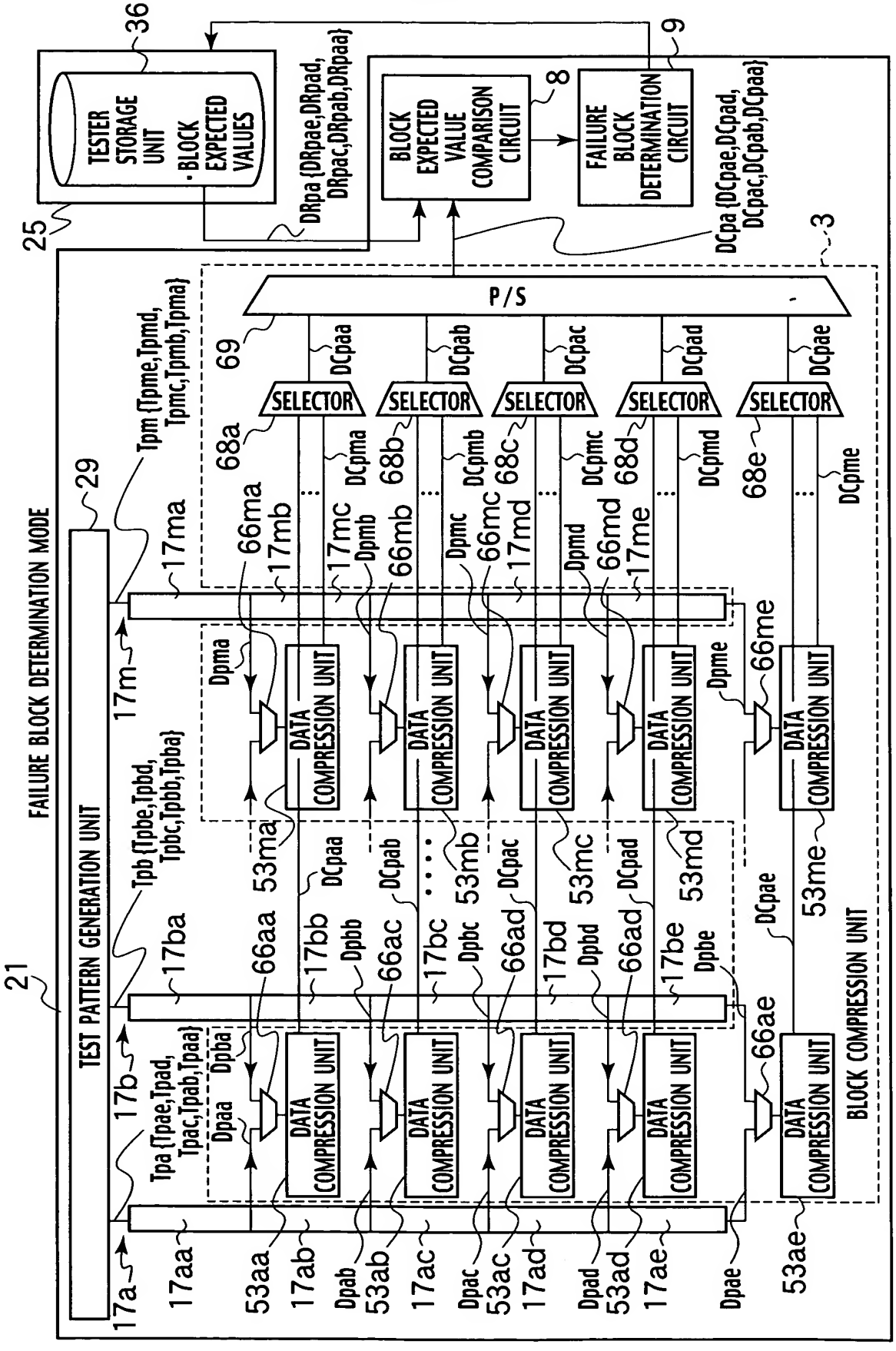

TESTER STORAGE UNIT
· BLOCK EXPECTED VALUES
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
FAILURE BLOCK DETERMINATION CIRCUIT
DRpa {DRpae,DRpad, DRpac,DRpab,DRpaa}
DCpa {DCpae,DCpad, DCpac,DCpab,DCpaa}
P/S
SELECTOR
DATA COMPRESSION UNIT
FAILURE BLOCK DETERMINATION MODE
TEST PATTERN GENERATION UNIT
BLOCK COMPRESSION UNIT
Tpm {Tpme,Tpmd, Tpmc,Tpmb,Tpma}
Tpb {Tpbe,Tpbd, Tpbc,Tpbb,Tpba}
Tpa {Tpae,Tpad, Tpac,Tpab,Tpaa}

FIG. 28

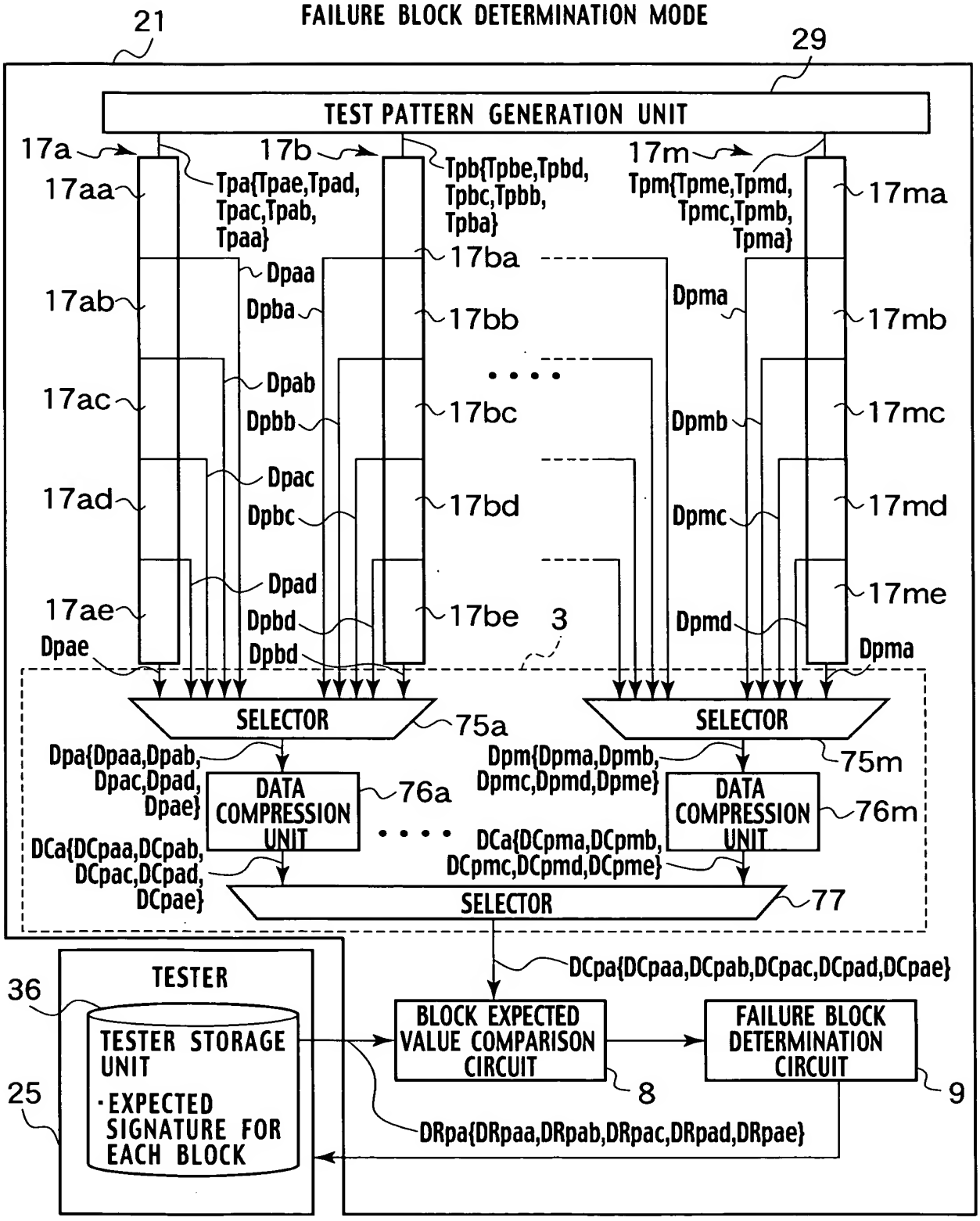

FAILURE BLOCK DETERMINATION MODE
21
29
TEST PATTERN GENERATION UNIT
17a
17b
17m
17aa
17ab
17ac
17ad
17ae
17ba
17bb
17bc
17bd
17be
17ma
17mb
17mc
17md
17me
Tpa{Tpae,Tpad, Tpac,Tpab, Tpaa}
Tpb{Tpbe,Tpbd, Tpbc,Tpbb, Tpba}
Tpm{Tpme,Tpmd, Tpmc,Tpmb, Tpma}
Dpaa
Dpba
Dpab
Dpbb
Dpac
Dpbc
Dpad
Dpbd
Dpma
Dpmb
Dpmc
Dpmd
Dpae
3
SELECTOR
75a
75m
Dpa{Dpaa,Dpab, Dpac,Dpad, Dpae}
Dpm{Dpma,Dpmb, Dpmc,Dpmd,Dpme}
DATA COMPRESSION UNIT
76a
76m
DCa{DCpaa,DCpab, DCpac,DCpad, DCpae}
DCa{DCpma,DCpmb, DCpmc,DCpmd,DCpme}
77
DCpa{DCpaa,DCpab,DCpac,DCpad,DCpae}
TESTER
36
TESTER STORAGE UNIT
·EXPECTED SIGNATURE FOR EACH BLOCK
25
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
8
FAILURE BLOCK DETERMINATION CIRCUIT
9
DRpa{DRpaa,DRpab,DRpac,DRpad,DRpae}

FIG. 29

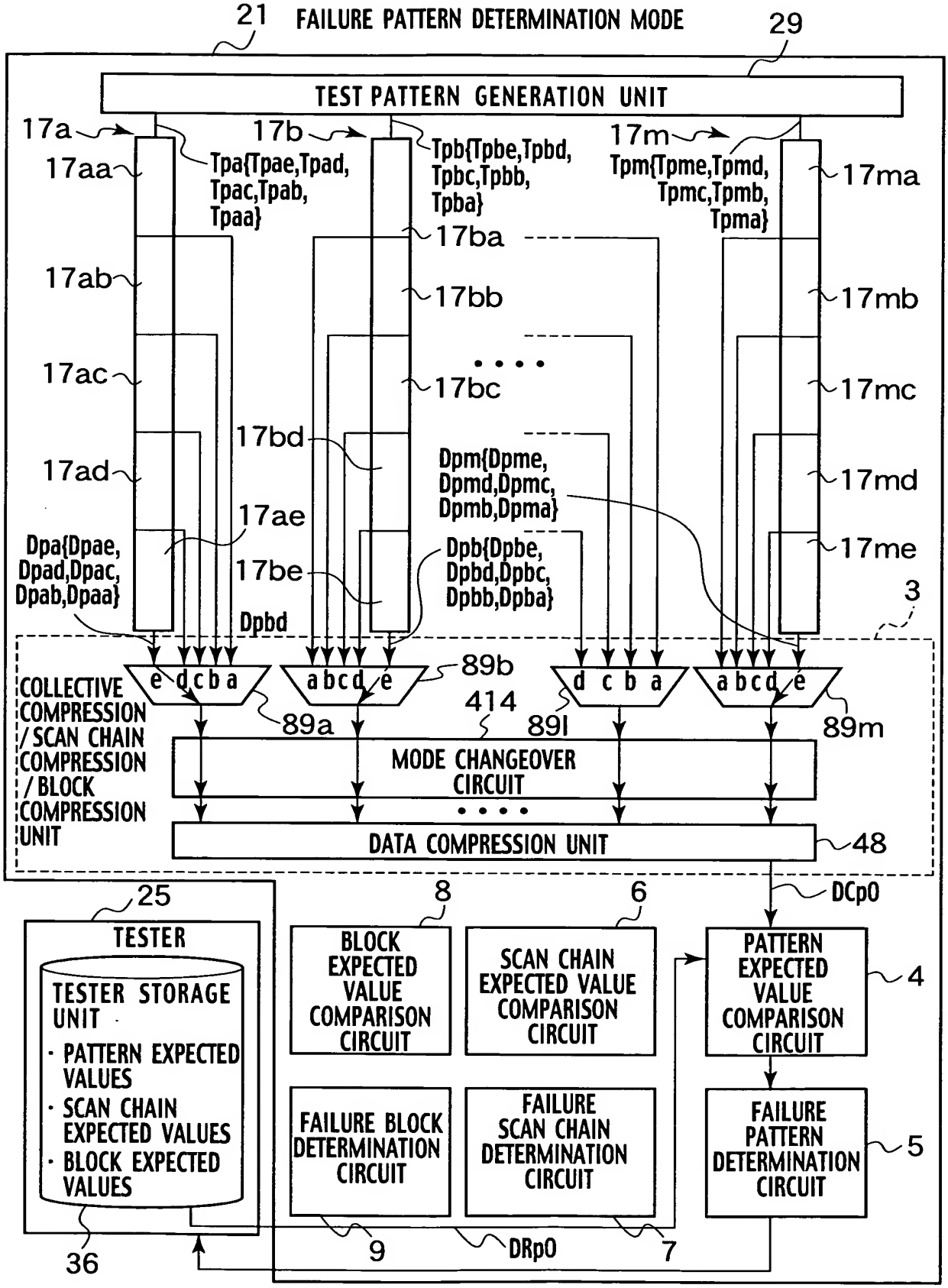

21
FAILURE PATTERN DETERMINATION MODE
29
TEST PATTERN GENERATION UNIT
17a
17aa
17ab
17ac
17ad
17ae
17be
17b
17ba
17bb
17bc
17bd
17m
17ma
17mb
17mc
17md
17me
Tpa{Tpae,Tpad, Tpac,Tpab, Tpaa}
Tpb{Tpbe,Tpbd, Tpbc,Tpbb, Tpba}
Tpm{Tpme,Tpmd, Tpmc,Tpmb, Tpma}
Dpa{Dpae, Dpad,Dpac, Dpab,Dpaa}
Dpbd
Dpb{Dpbe, Dpbd,Dpbc, Dpbb,Dpba}
Dpm{Dpme, Dpmd,Dpmc, Dpmb,Dpma}
3
COLLECTIVE COMPRESSION / SCAN CHAIN COMPRESSION / BLOCK COMPRESSION UNIT
e d c b a
a b c d e
d c b a
a b c d e
89b
89a
414
89l
89m
MODE CHANGEOVER CIRCUIT
DATA COMPRESSION UNIT
48
DCpO
25
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
36
8
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
6
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
4
FAILURE BLOCK DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
FAILURE PATTERN DETERMINATION CIRCUIT
5
9
DRpO
7

FIG. 30

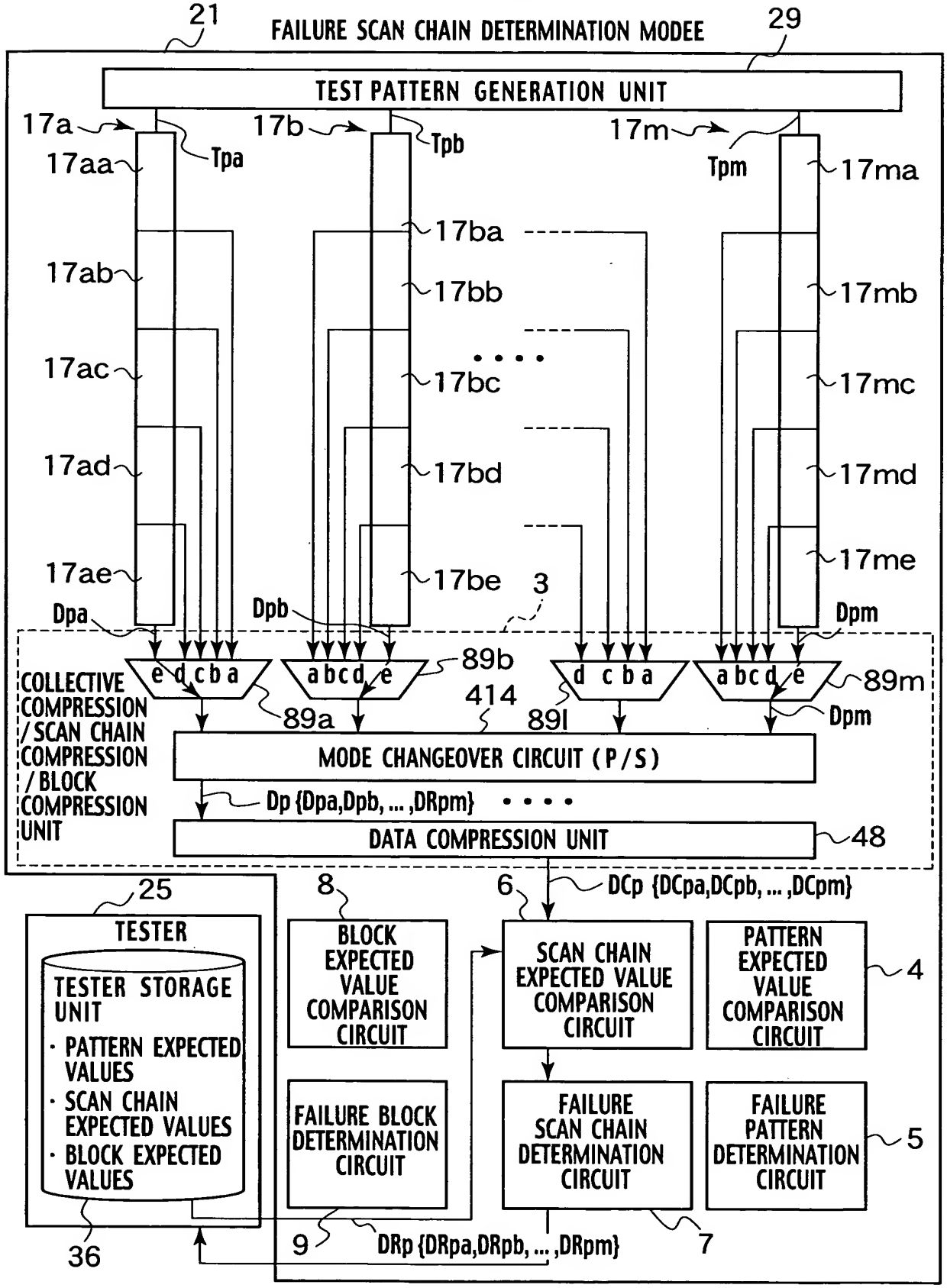

21
FAILURE SCAN CHAIN DETERMINATION MODEE
29
TEST PATTERN GENERATION UNIT
17a
17b
17m
Tpa
Tpb
Tpm
17aa
17ma
17ba
17ab
17bb
17mb
17ac
17bc
17mc
17ad
17bd
17md
17ae
17be
17me
3
Dpa
Dpb
Dpm
e d c b a
a b c d e
d c b a
a b c d e
89b
89m
414
89a
89l
Dpm
COLLECTIVE COMPRESSION / SCAN CHAIN COMPRESSION / BLOCK COMPRESSION UNIT
MODE CHANGEOVER CIRCUIT (P/S)
Dp {Dpa,Dpb, ... ,DRpm}
DATA COMPRESSION UNIT
48
25
8
6
DCp {DCpa,DCpb, ... ,DCpm}
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
4
FAILURE BLOCK DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
FAILURE PATTERN DETERMINATION CIRCUIT
5
36
9
DRp {DRpa,DRpb, ... ,DRpm}
7

FIG. 31

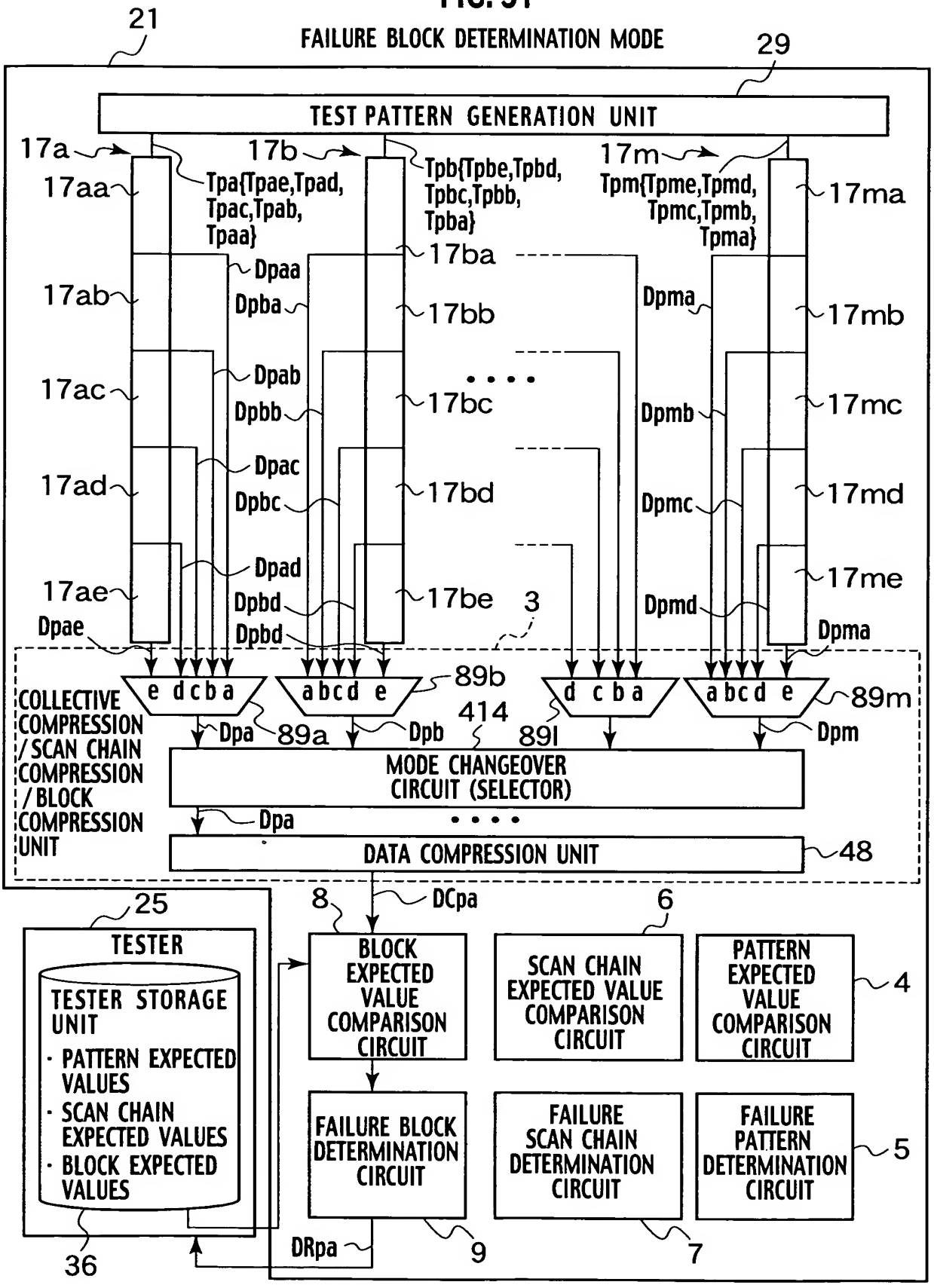

21
FAILURE BLOCK DETERMINATION MODE
29
TEST PATTERN GENERATION UNIT
17a
17b
17m
17aa
Tpa{Tpae,Tpad, Tpac,Tpab, Tpaa}
Tpb{Tpbe,Tpbd, Tpbc,Tpbb, Tpba}
Tpm{Tpme,Tpmd, Tpmc,Tpmb, Tpma}
17ma
17ba
Dpaa
17ab
Dpba
17bb
Dpma
17mb
Dpab
17ac
Dpbb
17bc
Dpmb
17mc
Dpac
17ad
Dpbc
17bd
Dpmc
17md
Dpad
17ae
Dpbd
17be
3
Dpmd
17me
Dpae
Dpbd
Dpma
e d c b a
a b c d e
d c b a
a b c d e
89b
89m
COLLECTIVE COMPRESSION / SCAN CHAIN COMPRESSION / BLOCK COMPRESSION UNIT
Dpa
89a
Dpb
414
89l
Dpm
MODE CHANGEOVER CIRCUIT (SELECTOR)
Dpa
DATA COMPRESSION UNIT
48
25
8
DCpa
6
TESTER
TESTER STORAGE UNIT
· PATTERN EXPECTED VALUES
· SCAN CHAIN EXPECTED VALUES
· BLOCK EXPECTED VALUES
BLOCK EXPECTED VALUE COMPARISON CIRCUIT
SCAN CHAIN EXPECTED VALUE COMPARISON CIRCUIT
PATTERN EXPECTED VALUE COMPARISON CIRCUIT
4
FAILURE BLOCK DETERMINATION CIRCUIT
FAILURE SCAN CHAIN DETERMINATION CIRCUIT
FAILURE PATTERN DETERMINATION CIRCUIT
5
DRpa
9
7
36

FIG. 32

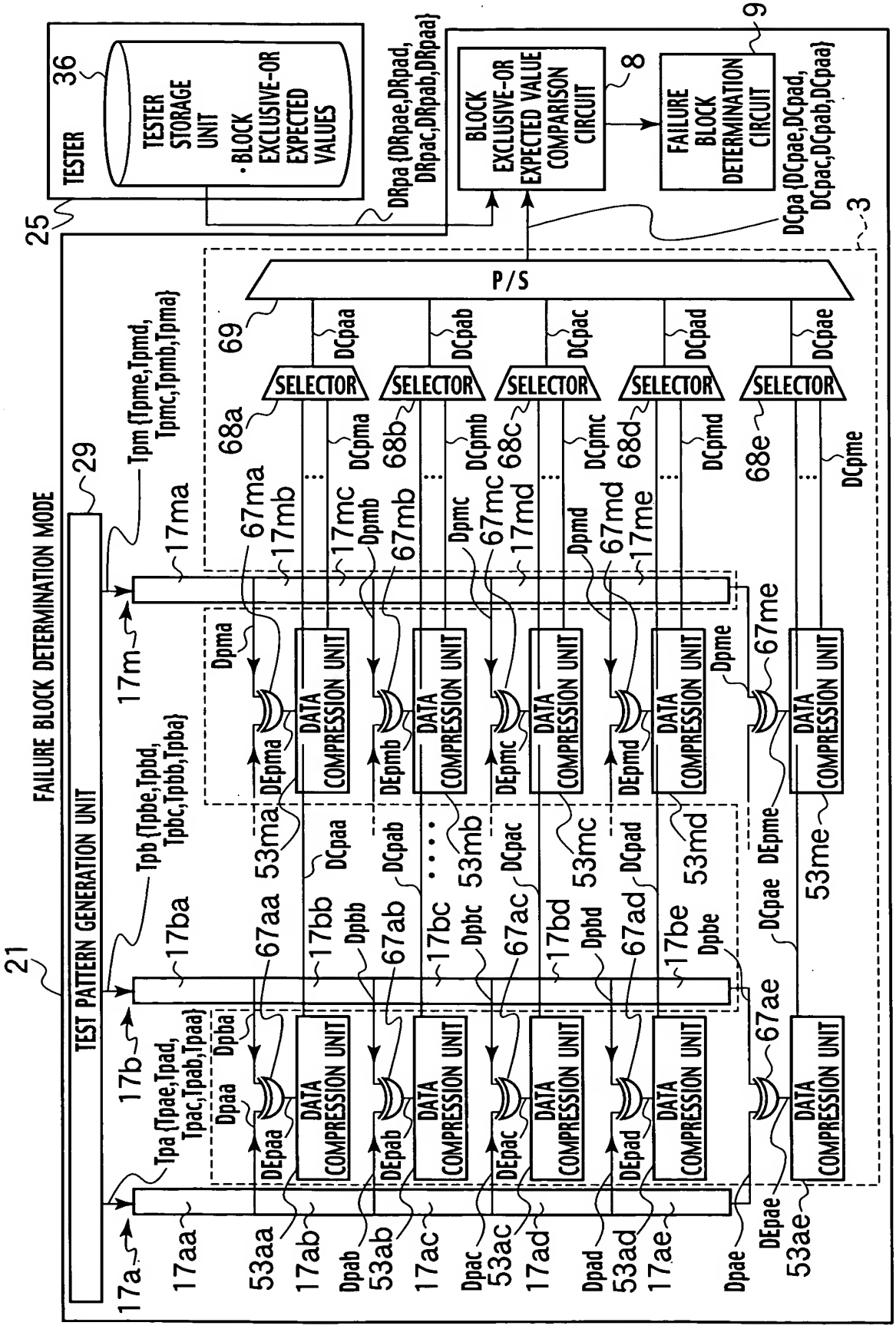

TESTER
36
TESTER STORAGE UNIT
· BLOCK EXCLUSIVE-OR EXPECTED VALUES
25
DRpa {DRpae,DRpad, DRpac,DRpab,DRpaa}
BLOCK EXCLUSIVE-OR EXPECTED VALUE COMPARISON CIRCUIT
8
FAILURE BLOCK DETERMINATION CIRCUIT
9
DCpa {DCpae,DCpad, DCpac,DCpab,DCpaa}
3
P/S
69
SELECTOR
68a
68b
68c
68d
68e
DCpaa
DCpab
DCpac
DCpad
DCpae
DCpma
DCpmb
DCpmc
DCpmd
DCpme
FAILURE BLOCK DETERMINATION MODE
29
TEST PATTERN GENERATION UNIT
21
Tpm {Tpme,Tpmd, Tpmc,Tpmb,Tpma}
Tpb {Tpbe,Tpbd, Tpbc,Tpbb,Tpba}
Tpa {Tpae,Tpad, Tpac,Tpab,Tpaa}
17a
17b
17m
17ma
17mb
17mc
17md
17me
17ba
17aa
17ab
17ac
17ad
17ae
17bb
17bc
17bd
17be
67ma
67mb
67mc
67md
67me
67aa
67ab
67ac
67ad
67ae
Dpma
Dpmb
Dpmc
Dpmd
Dpme
Dpaa
Dpba
Dpbb
Dpbc
Dpbd
Dpbe
Dpab
Dpac
Dpad
Dpae
DEpma
DEpmb
DEpmc
DEpmd
DEpme
DEpaa
DEpab
DEpac
DEpad
DEpae
DATA COMPRESSION UNIT
53ma
53mb
53mc
53md
53me
53aa
53ab
53ac
53ad
53ae

FIG. 33

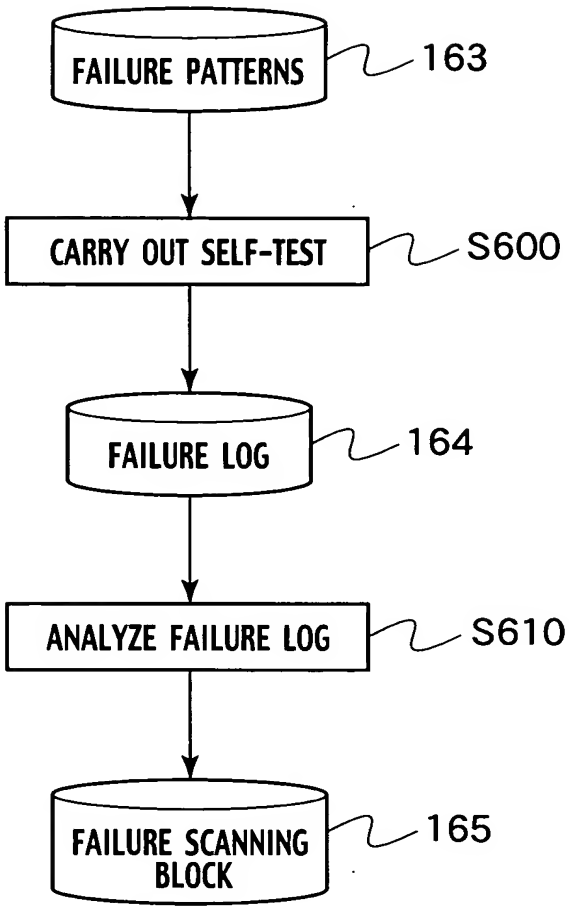

FAILURE PATTERNS
163
CARRY OUT SELF-TEST
S600
FAILURE LOG
164
ANALYZE FAILURE LOG
S610
FAILURE SCANNING BLOCK
165

FIG. 34

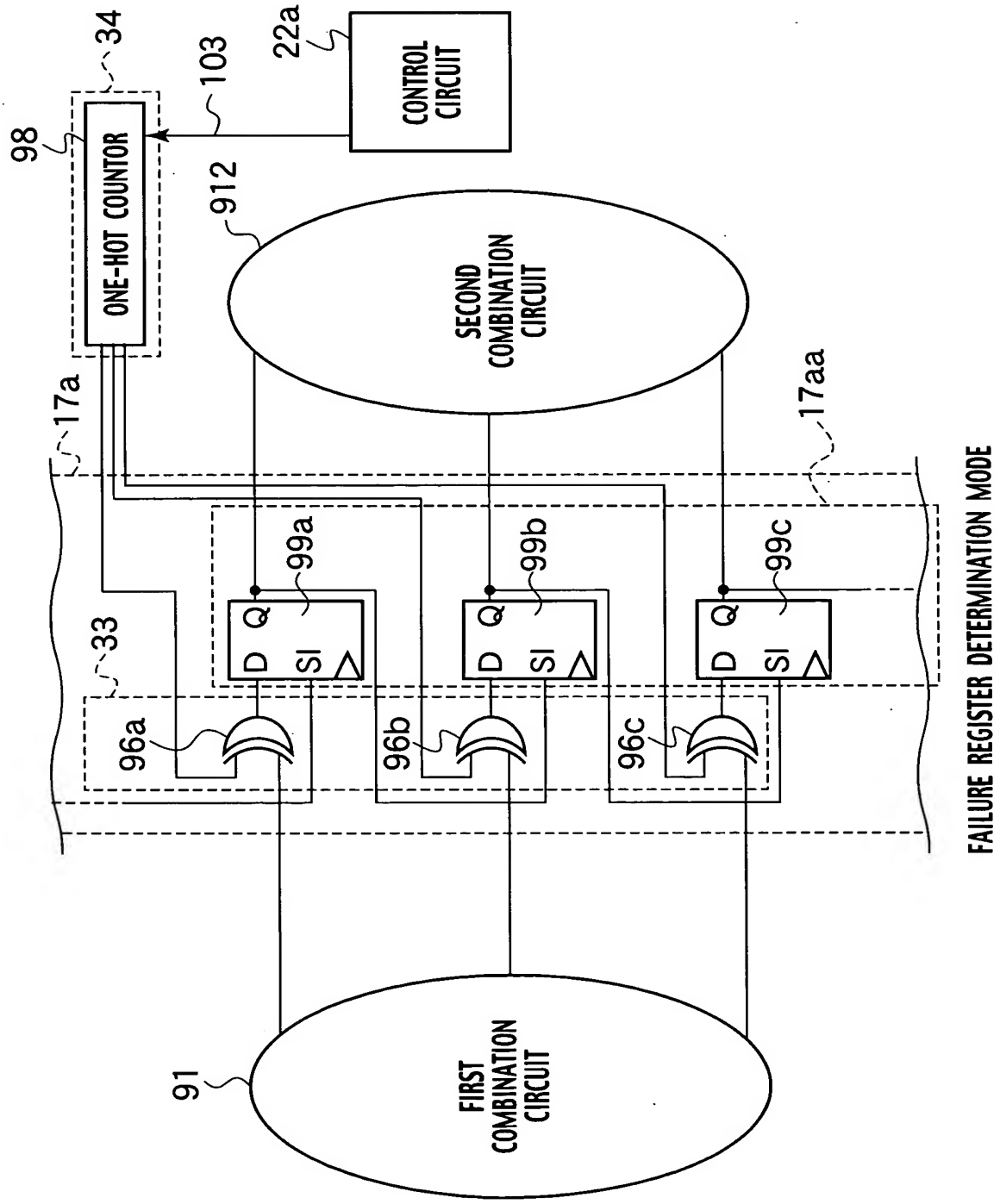

34
98
ONE-HOT COUNTOR
103
22a
CONTROL CIRCUIT
912
SECOND COMBINATION CIRCUIT
17a
17aa
33
99a
99b
99c
D
Q
SI
96a
96b
96c
91
FIRST COMBINATION CIRCUIT
FAILURE REGISTER DETERMINATION MODE

FIG. 35

	XOR (96a)	XOR (96b)	XOR (96c)	• · · · •
RESET	0	0	0	0 · · · 0
SET 1	1	0	0	0 · · · 0
SET 2	0	1	0	0 · · · 0
SET 3	0	0	1	0 · · · 0
• ⋮ •	0 ⋮ 0	0 ⋮ 0	0 ⋮ 0	1 · · · 0 ⋮ ⋱ 0 1

FIG. 36

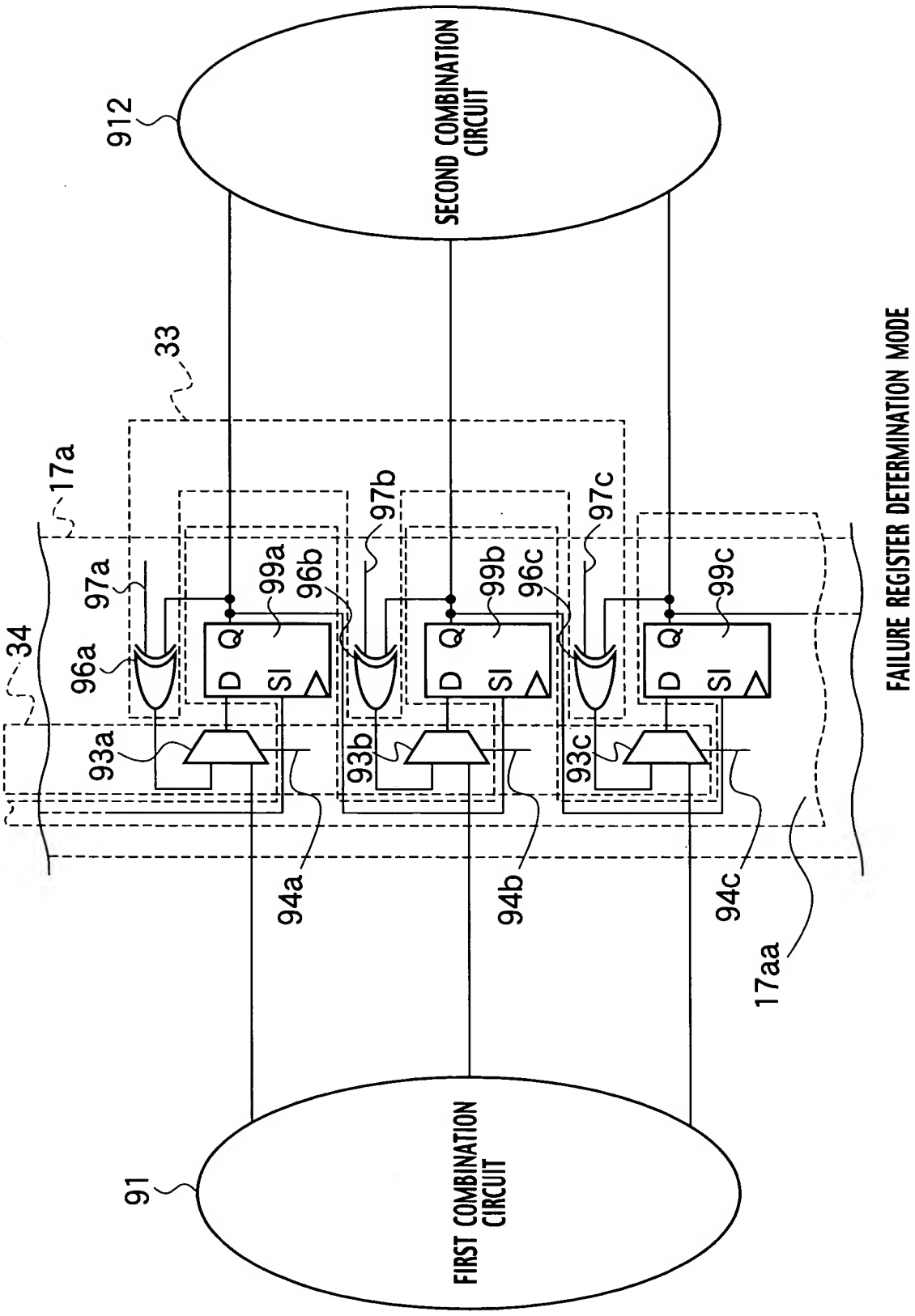

912
SECOND COMBINATION CIRCUIT
33
17a
34
97a
96a
99a
96b
97b
99b
96c
97c
99c
Q
D
SI
93a
93b
93c
94a
94b
94c
17aa
91
FIRST COMBINATION CIRCUIT
FAILURE REGISTER DETERMINATION MODE

FIG. 37

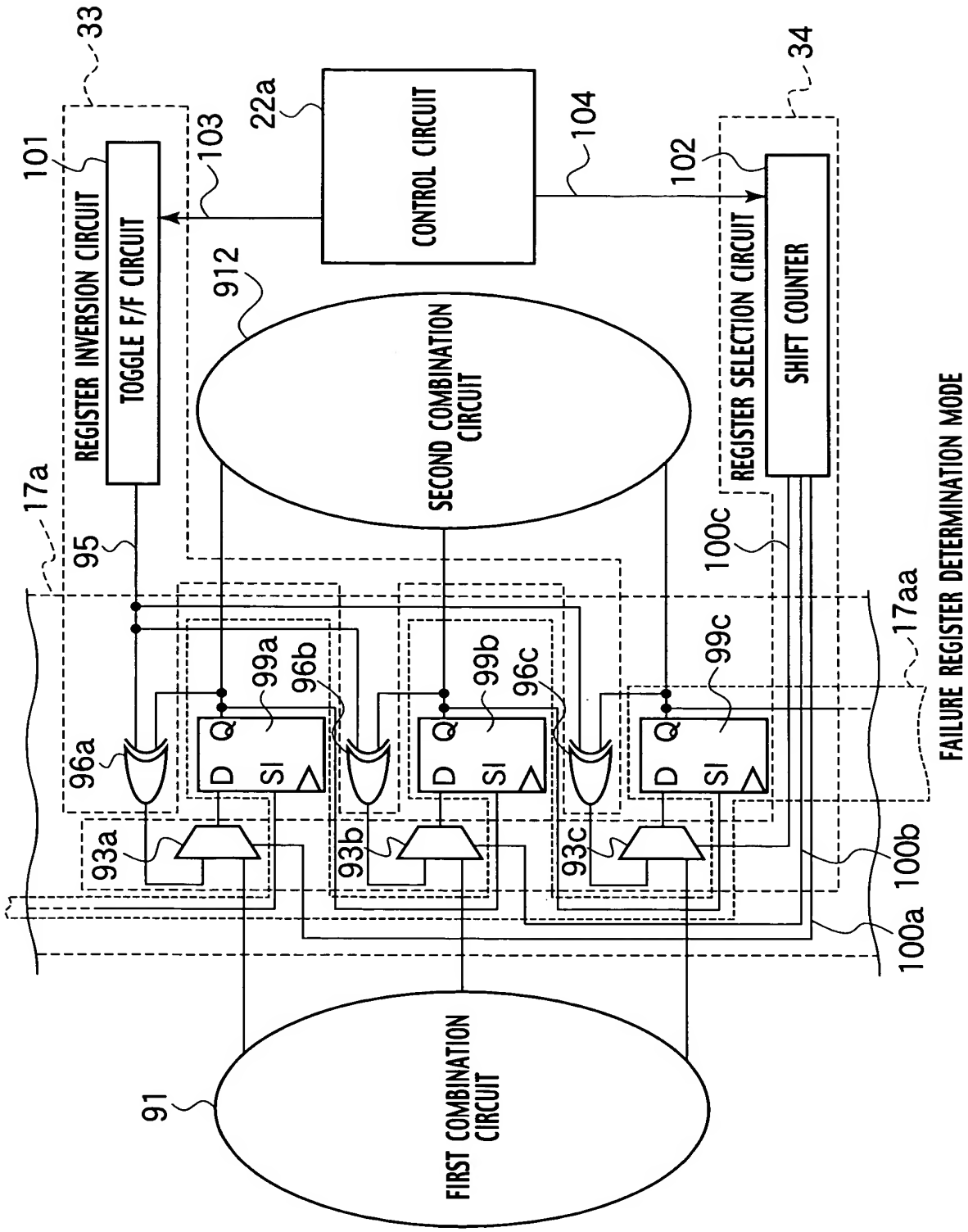

33
101
REGISTER INVERSION CIRCUIT
TOGGLE F/F CIRCUIT
103
22a
CONTROL CIRCUIT
104
102
34
REGISTER SELECTION CIRCUIT
SHIFT COUNTER
912
SECOND COMBINATION CIRCUIT
17a
95
100c
17aa
99a
96b
99b
96c
99c
96a
Q
D
SI
93a
93b
93c
100b
100a
FAILURE REGISTER DETERMINATION MODE
91
FIRST COMBINATION CIRCUIT

FIG. 38

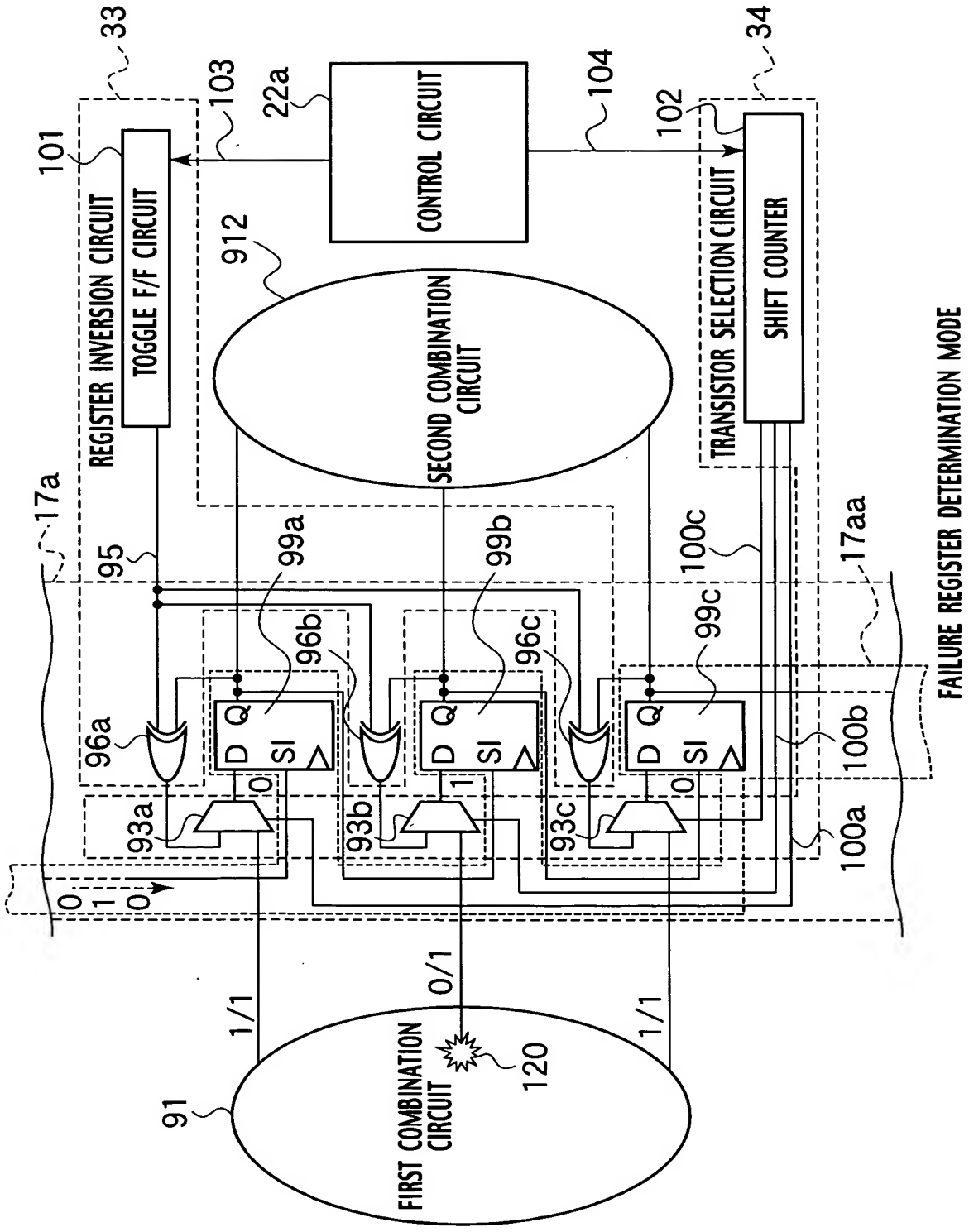

33
101
REGISTER INVERSION CIRCUIT
TOGGLE F/F CIRCUIT
103
22a
CONTROL CIRCUIT
104
102
34
TRANSISTOR SELECTION CIRCUIT
SHIFT COUNTER
912
SECOND COMBINATION CIRCUIT
17a
95
99a
99b
100c
17aa
96a
96b
96c
99c
D
Q
SI
100b
93a
93b
93c
100a
0
1
0/1
1/1
91
FIRST COMBINATION CIRCUIT
120
FAILURE REGISTER DETERMINATION MODE

FIG. 39

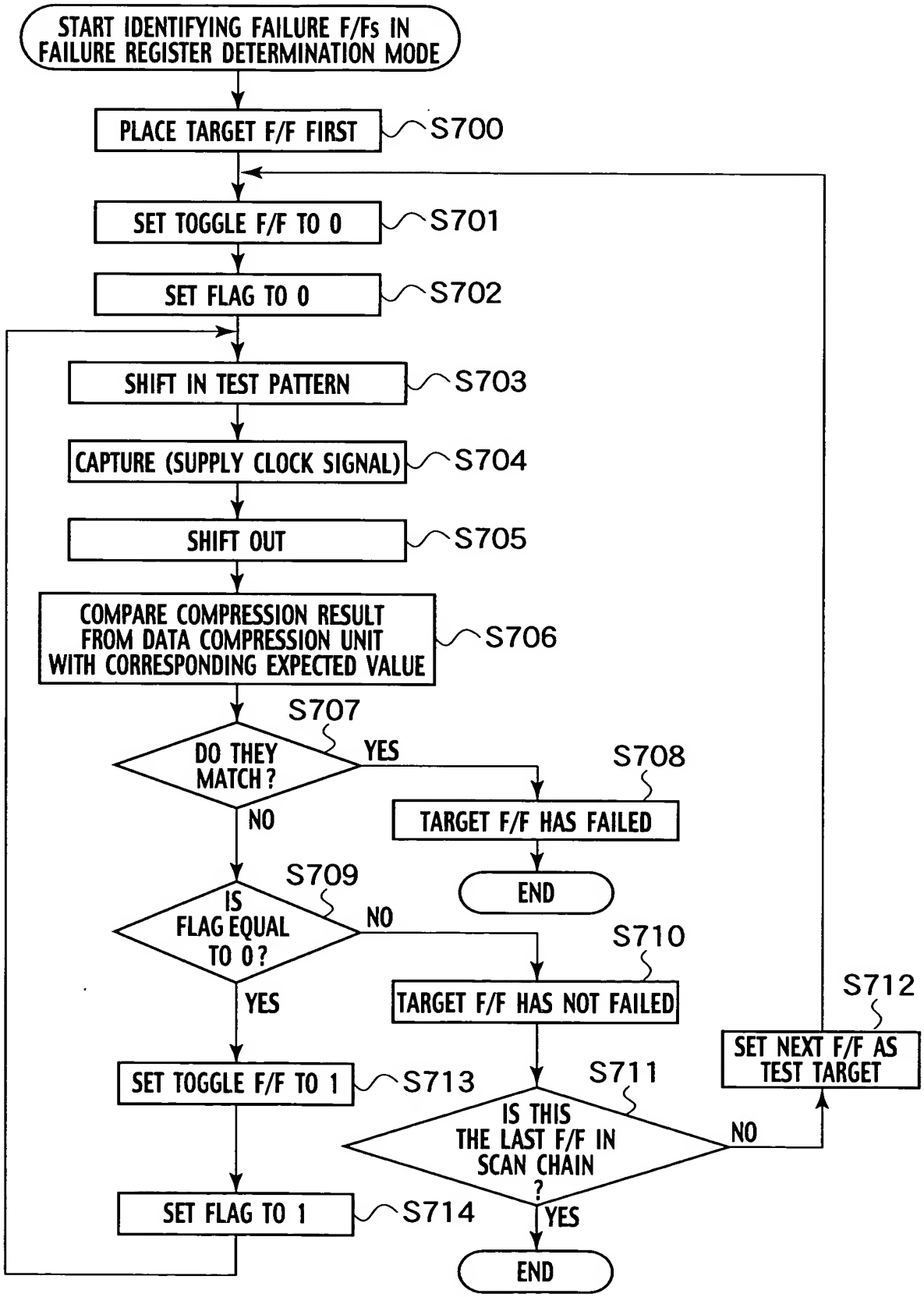

START IDENTIFYING FAILURE F/Fs IN FAILURE REGISTER DETERMINATION MODE
PLACE TARGET F/F FIRST
S700
SET TOGGLE F/F TO 0
S701
SET FLAG TO 0
S702
SHIFT IN TEST PATTERN
S703
CAPTURE (SUPPLY CLOCK SIGNAL)
S704
SHIFT OUT
S705
COMPARE COMPRESSION RESULT FROM DATA COMPRESSION UNIT WITH CORRESPONDING EXPECTED VALUE
S706
S707
DO THEY MATCH?
YES
NO
S708
TARGET F/F HAS FAILED
END
S709
IS FLAG EQUAL TO 0?
NO
YES
S710
TARGET F/F HAS NOT FAILED
S712
SET NEXT F/F AS TEST TARGET
SET TOGGLE F/F TO 1
S713
S711
IS THIS THE LAST F/F IN SCAN CHAIN ?
NO
YES
SET FLAG TO 1
S714
END

FIG. 40

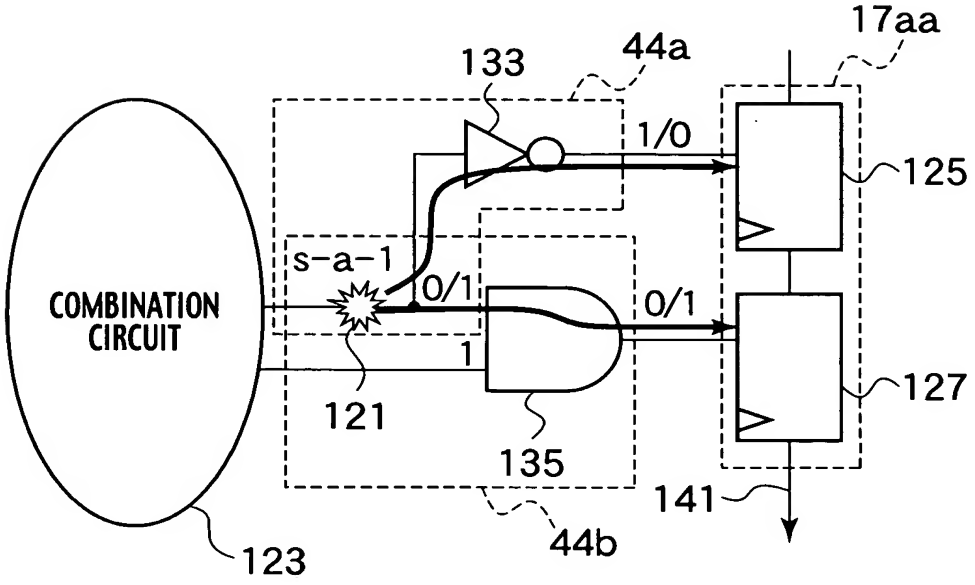

17aa
133
44a
1/0
125
COMBINATION CIRCUIT
s-a-1
0/1
0/1
1
127
121
135
141
44b
123

FIG. 41

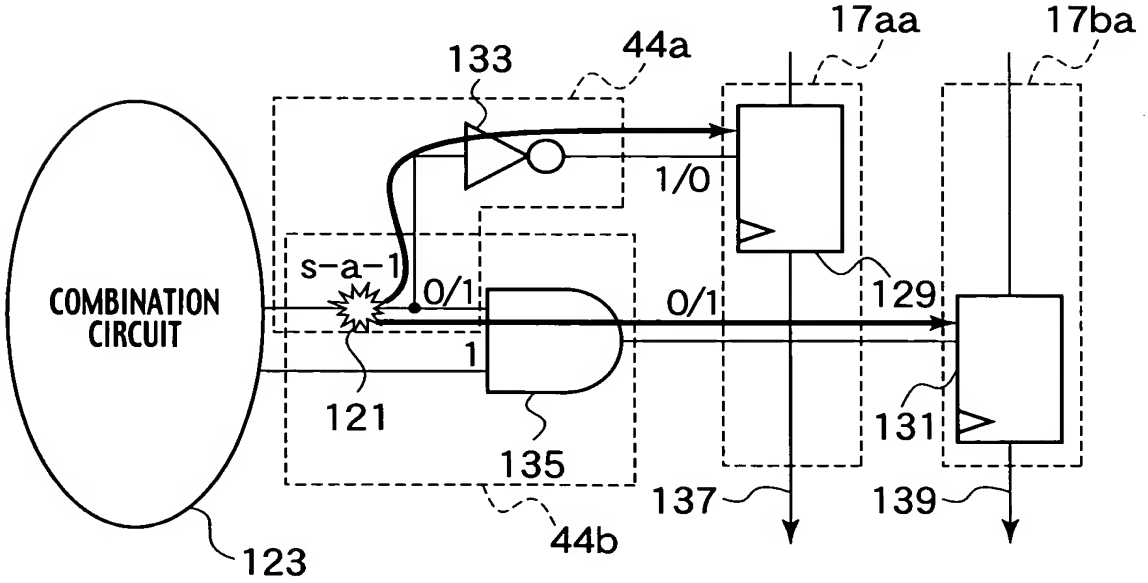

17aa
17ba
133
44a
1/0
COMBINATION CIRCUIT
s-a-1
0/1
0/1
129
1
121
131
135
137
139
44b
123

FIG. 42

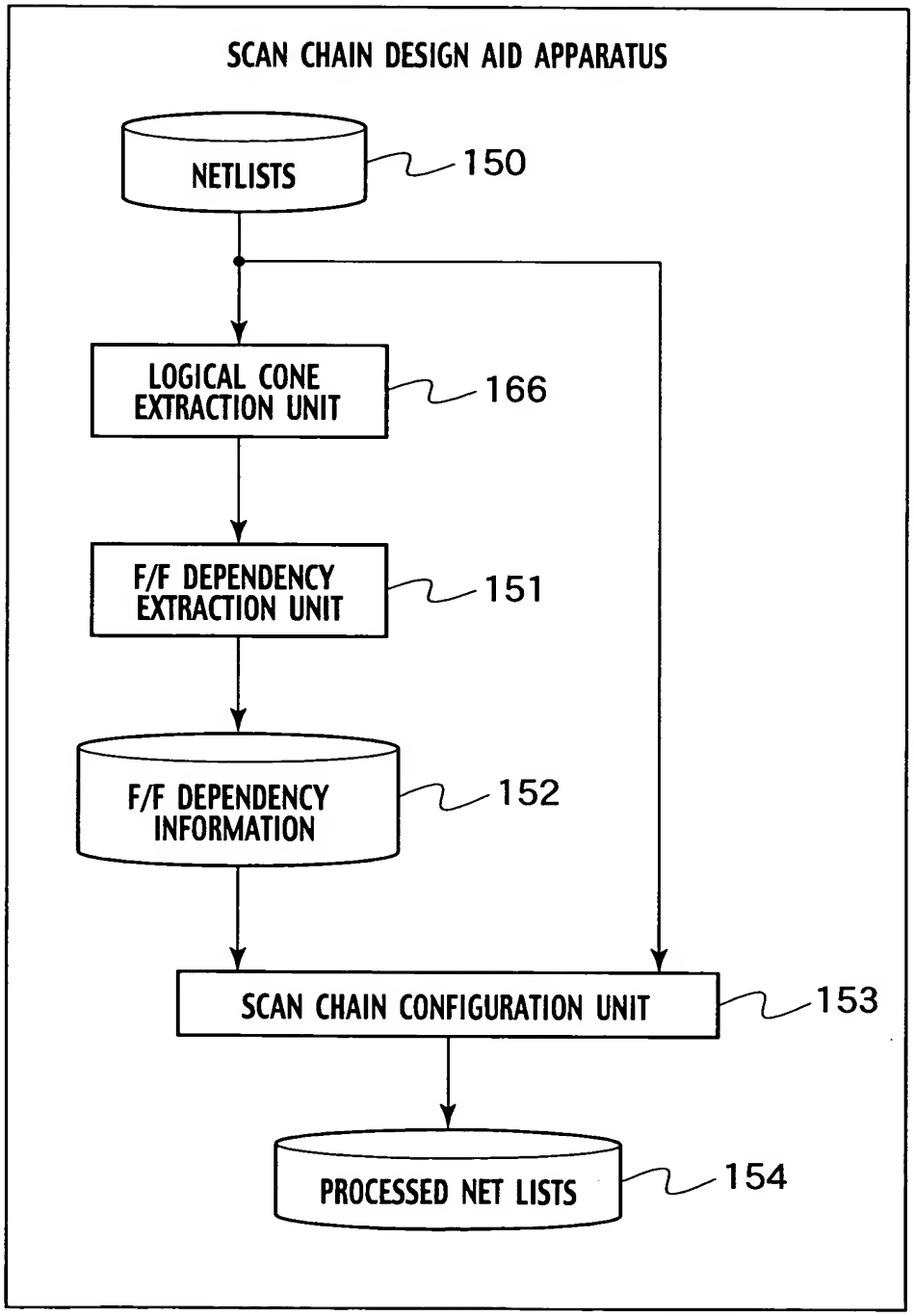

SCAN CHAIN DESIGN AID APPARATUS
NETLISTS
150
LOGICAL CONE EXTRACTION UNIT
166
F/F DEPENDENCY EXTRACTION UNIT
151
F/F DEPENDENCY INFORMATION
152
SCAN CHAIN CONFIGURATION UNIT
153
PROCESSED NET LISTS
154

FIG. 43

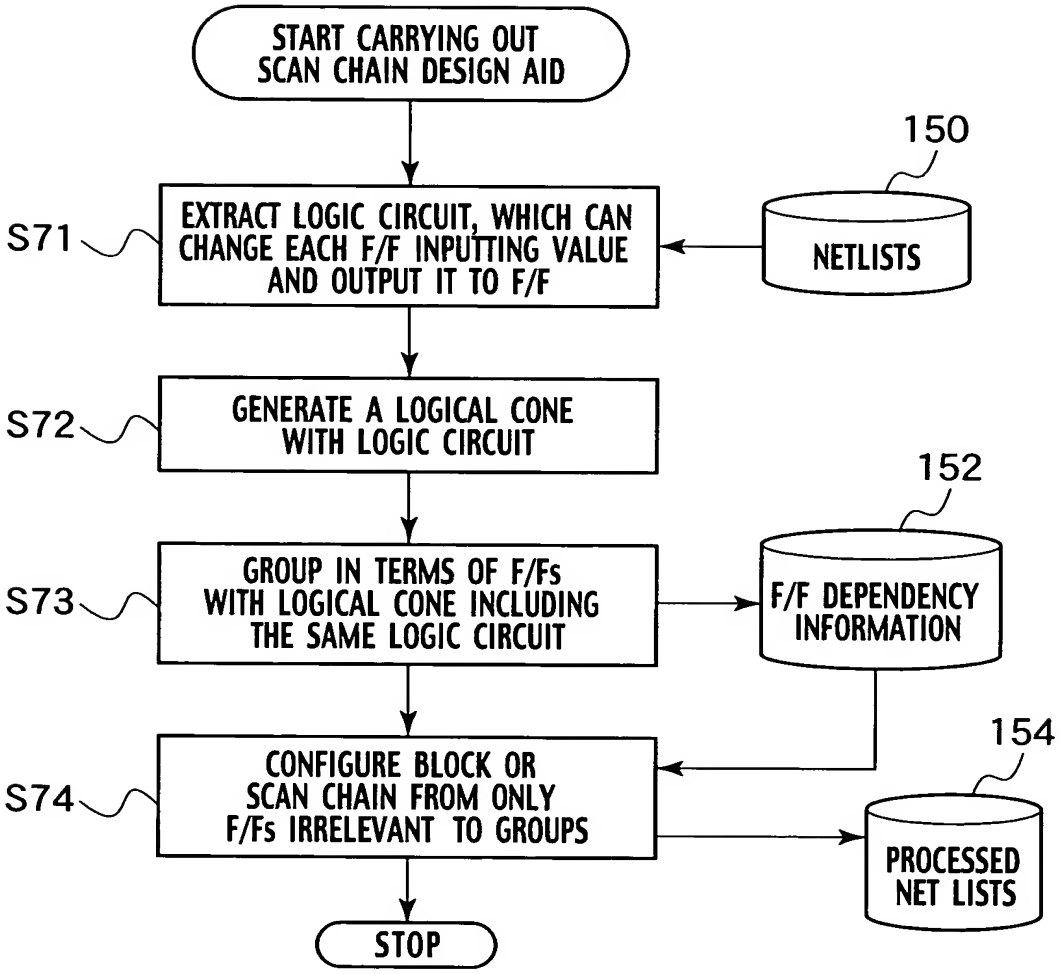

START CARRYING OUT SCAN CHAIN DESIGN AID
150
S71
EXTRACT LOGIC CIRCUIT, WHICH CAN CHANGE EACH F/F INPUTTING VALUE AND OUTPUT IT TO F/F
NETLISTS
S72
GENERATE A LOGICAL CONE WITH LOGIC CIRCUIT
152
S73
GROUP IN TERMS OF F/Fs WITH LOGICAL CONE INCLUDING THE SAME LOGIC CIRCUIT
F/F DEPENDENCY INFORMATION
154
S74
CONFIGURE BLOCK OR SCAN CHAIN FROM ONLY F/Fs IRRELEVANT TO GROUPS
PROCESSED NET LISTS
STOP

FIG. 44

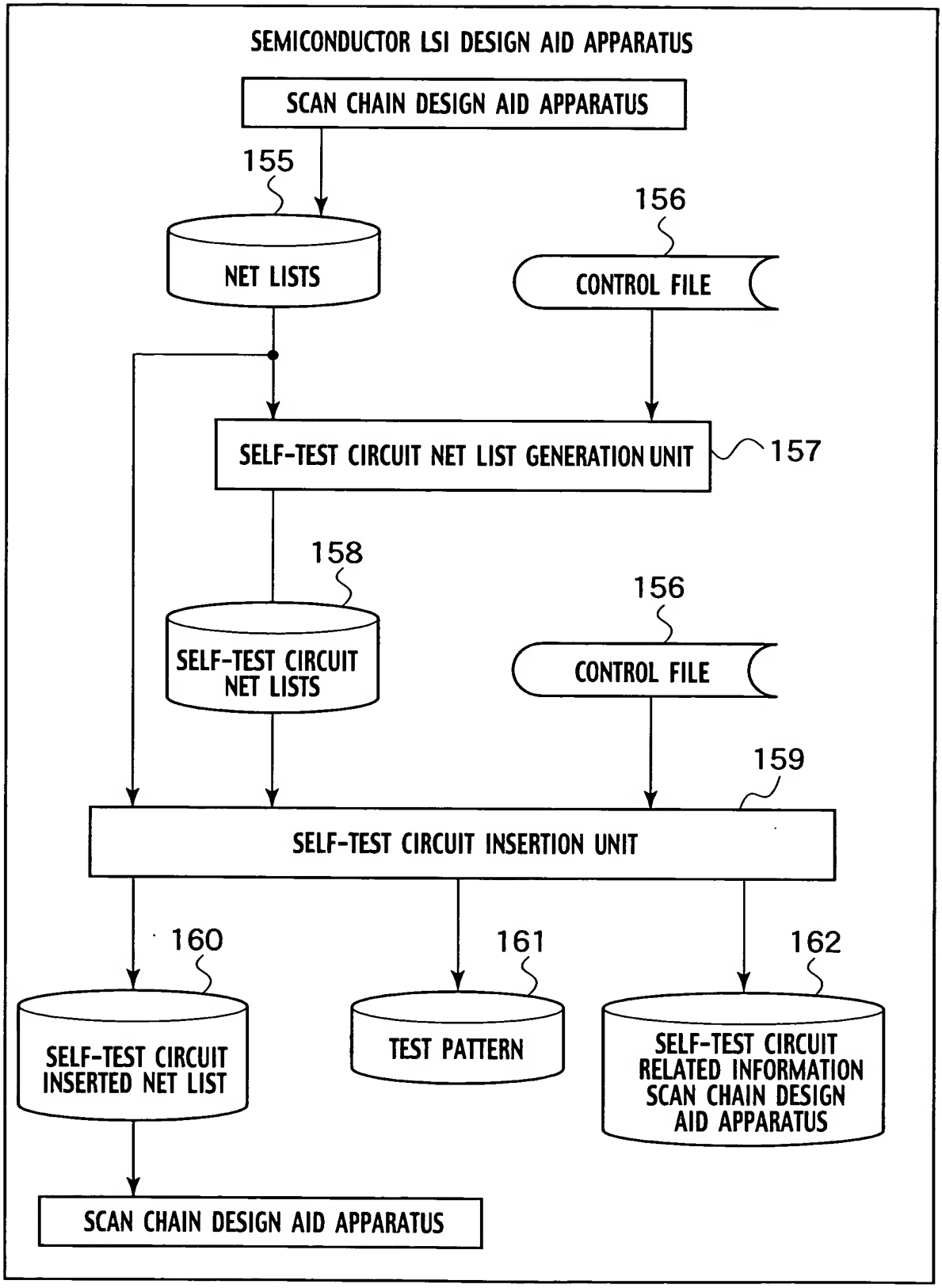
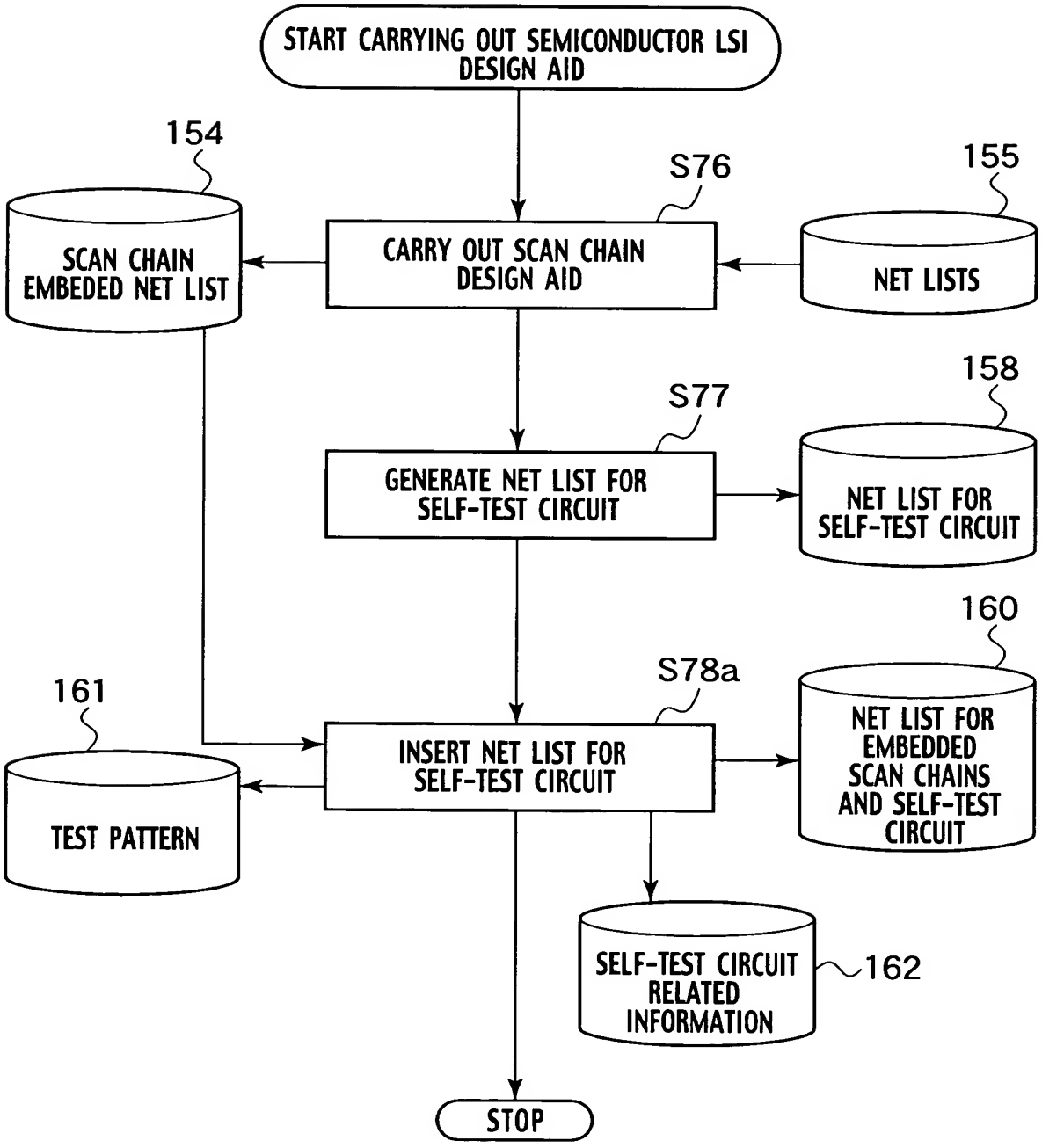

SEMICONDUCTOR LSI DESIGN AID APPARATUS
SCAN CHAIN DESIGN AID APPARATUS
155
NET LISTS
156
CONTROL FILE
SELF-TEST CIRCUIT NET LIST GENERATION UNIT
157
158
SELF-TEST CIRCUIT NET LISTS
156
CONTROL FILE
159
SELF-TEST CIRCUIT INSERTION UNIT
160
SELF-TEST CIRCUIT INSERTED NET LIST
161
TEST PATTERN
162
SELF-TEST CIRCUIT RELATED INFORMATION SCAN CHAIN DESIGN AID APPARATUS
SCAN CHAIN DESIGN AID APPARATUS

FIG. 45


START CARRYING OUT SEMICONDUCTOR LSI DESIGN AID
154
SCAN CHAIN EMBEDED NET LIST
S76
CARRY OUT SCAN CHAIN DESIGN AID
155
NET LISTS
S77
GENERATE NET LIST FOR SELF-TEST CIRCUIT
158
NET LIST FOR SELF-TEST CIRCUIT
160
S78a
161
TEST PATTERN
INSERT NET LIST FOR SELF-TEST CIRCUIT
NET LIST FOR EMBEDDED SCAN CHAINS AND SELF-TEST CIRCUIT
SELF-TEST CIRCUIT RELATED INFORMATION
162
STOP